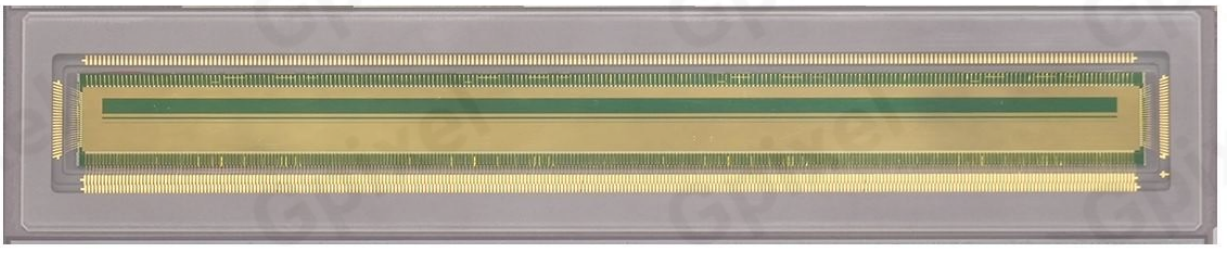
GLT5016BSI

16416 x 256 Stages BSI CMOS TDI Image Sensor



Preliminary Datasheet V0.3.5

Features

- 2 photosensitive bands: P1 band and P2 band.
- Effective resolution
  - P1 band: 16416 pixels x 256 stages
  - P2 band: 16416 pixels x 32 stages
- Single band Max. line frequency
  - 500kHz @ 10bit/12bit
- Pixel size: 5μm x 5μm
- Charge domain BSI TDI
- High speed and high sensitivity
- External Triggering
- QE: 70.76% @266nm
- Functions
  - Horizontal image flipping
  - Channel multiplexing
  - Dual band HDR mode
- 10/12bit ADC depth
- On chip sequencer and SPI control

Applications

- FPD Inspection
- PCB Inspection
- Wafer (Semiconductor) Inspection
- Fluorescence Imaging
- Digital Pathology

Description

GLT5016BSI is a Backside illuminated (BSI), Time delay integration (TDI), charge domain CMOS image sensor with 5μm pixels and 16416 effective resolutions. The sensor has two photosensitive bands, 256 stages and 32 stages respectively enabling a high dynamic range (HDR) imaging mode, which is designed to meet the needs of high speed and low light applications by maximizing sensitivity with state-of-art BSI scientific CMOS technology.

GLT5016BSI sensor integrates an on-chip sequencer, supports channel multiplexing and selectable 2 scan directions (Forward and Reverse). It is assembled in a 415-pin μPGA ceramic package for reliability and good heat dissipation.

GLT5016BSI comes in 2 spectrum variants: a UV-optimized with high QE below 300 nm and a visible and NIR range optimized version.

Specifications

Parameter	Value
Photosensitive area	P1: 82.08mm x 1.28mm P2: 82.08mm x 0.16mm
Pixel size	5μm x 5μm
Number of effective pixels	P1: 16416(H) x 256(V) P2: 16416(H) x 32(V)
Effective optical black columns	80(left) + 80(right)
Input clock rate	40MHz @ 10bit single band 80MHz @ 12bit single band
Line frequency	500kHz @ 12bit/10bit single band
Full well capacity (FWC)	15.2ke$^-$ @ P1 12bit single band 16.3ke$^-$ @ P1 10bit single band
Temporal noise	7.5e$^-$ @ P1 12bit single band 15.3e$^-$ @ P1 10bit single band
Intra-scene dynamic range	66.1dB @ P1 12bit single band 60.5dB @ P1 10bit single band
Charge transfer efficiency (CTE)	> 0.99999 @ P1 10/12bit single band
Dark Current (15 °C die temperature)	0.97ke$^-$/s/pixel @ P1 10/12bit single band
PRNU	0.3% @ P1 10/12bit single band
Max. data rate	103.68Gbps @ 12bit single band 86.40Gbps @ 10bit single band
Supply voltage	3.3V for analog, 1.65V for ADC, 1.6V for digital
Output format	108 x Sub-LVDS for effective data output, per sub-LVDS lane runs at 960Mbps @ 12bit single band 72 x Sub-LVDS for effective data output, per sub-LVDS lane runs at 1.2Gbps @ 10bit single band 2 x Sub-LVDS for OB data output 4 x Sub-LVDS for DDR clock output
Power consumption	<6.6W @ P1 12bit 500kHz line rate <6.3W @ P1 10bit 500kHz line rate
Chroma	Mono
Package	μPGA 415 pins

Revision History

Version	Date(dd/mm/yyyy)	Comment
V0.1	13/06/2024	First release
V0.1.1	18/06/2024	1. Update Specifications. 2. Update Table 2 and note in DC Characteristics 3. Update Figure 27 in Clock System. 4. Update Figure 28 in Trigger and Sensor Line Time. 5. Update Figure 34 in SYNC Code 6. Update Figure 36 and Figure 37 in TDI Pushing Scan Direction. 7. Update Figure 45 in OTP Data Description.
V0.1.2	16/08/2024	1. Update office location.
V0.1.3	21/10/2024	1. Update Figure 22 in Sub-LVDS Inputs/Outputs 2. Update Figure 3 in Optical Center & Temperature Sensor. 3. Add note in Pin Description. 4. Delete note 2 of Table 5 in AC Characteristics. 5. Update Figure 21 in Digital I/O and Clock inputs. 6. Add TRIG signal in Figure 23 and update note 2 in Power On/Off Sequence. 7. Update Description. 8. Update Figure 3 in Optical Center & Temperature Sensor. 9. Update No.58 VPP in Table 1 in Pin Description. 10. Add VPP and note in Table 2 in DC Characteristics. 11. Add connection of VPP in Figure 17 and note in Digital Power Connections. 12. Update description of VRPC/VRINIT in Table 1 in Pin Description. 13. Update Table 5 in AC Characteristics. 14. Update byte number of register in Register Communication Timing. 15. Update register name in Figure 27 in Clock System. 16. Update name in Table 17 in Data Interface Training. 17. Update Figure 31 in Line Format. 18. Delete note in Pixel Band Selection. 19. Add note in Test Image. 20. Update figure name of Figure 41 in Test Image. 21. Delete note in Sub-LVDS Output. 22. Add Figure 32 in Line Format. 23. Add note in Sensor Operation Overview. 24. Update Register Map. 25. Update table in Absolute Maximum Rating. 26. Update Figure 2 and note in Package Outline. 27. Update Figure 39 in Image Flipping. 28. Udpate Figure 22 in Sub-LVDS Inputs/Outputs. 29. Add Optical Marker. 30. Update note of Figure 23 in Power On/Off Sequence.
V0.2.0	05/12/2024	1. Update Figure 2 and note in Package Outline.

		2. Add note of Figure 34 in SYNC Code. 3. Update Figure 41 in Test Image. 4. Add note in Trigger and Sensor Line Time. 5. Update address of TEMP_DATA in Digital Temperature Sensor. 6. Update SPI WRITE. 7. Update Figure 27 in Clock System. 8. Update data rate in Specifications and Channel Multiplexing. 9. Update Applications. 10. Update Description. 11. Update Specifications. 12. Update Absolute Maximum Rating. 13. Update Table 1 in Pin Description. 14. Delete note for test of Table 1 in Pin Description. 15. Update Figure 5 in Pixel Arrangement. 16. Update Figure 6 in Internal Block Diagram. 17. Update Table 2 and note in DC Characteristics. 18. Update DDR clock and data rate in Table 5 in AC Characteristics. 19. Update Table 6 in Power Consumption. 20. Update Table 10 in Register Map. 21. Update Image Data Output Format. 22. Update Figure 42 in Digital Temperature Sensor. 23. Update Line Rate Calculation. 24. Update Table 20 and Figure 34 in SYNC Code. 25. Update Pixel Band Selection. 26. Update Figure 18 in Array Supply Connections. 27. Update Figure 21 and delete note in Digital I/O and Clock inputs. 28. Update Figure 32 and description below in Line Format. 29. Update Table 16 in Internal Line Time. 30. Update Figure 35 and description in Area Mode. 31. Delete note in Test Image. 32. Update Product Ordering Information. 33. Update Figure 17 and note in Digital Power Connections. 34. Update Figure 23 in Power On/Off Sequence. 35. Update Figure 39 in Image Flipping. 36. Update Figure 27 and Table 14 in Clock System. 37. Update Figure 29 and description in Block Based Readout. 38. Update Storage Condition and Handling. 39. Update Figure 41 in Test Image. 40. Update Sub-LVDS Output and Clock Channels. 41. Update Figure 22 in Sub-LVDS Inputs/Outputs. 42. Add location of analog temperature sensor in Figure 3 in Optical Center & Temperature Sensor. 43. Add sensor image in the cover sheet. 44. Update Features.

V0.3.0	30/12/2024	1. Delete Release Note for Preliminary Datasheet. 2. Update Description in Table 17 in Data Interface Training. 3. Update VDDIO voltage in Table 2 in DC Characteristics. 4. Update Table 3 and Table 4 in AC Characteristics. 5. Update Table 6 in Power Consumption. 6. Add Key Specification, Temporal Dark Noise Distribution, Spectral Sensitivity Characteristics and Dark Current with Different Die Temperature in Image Sensor Characteristics. 7. Update Table 10 in Register Map. 8. Add Analog Gain in Description of Various Functions. 9. Update Power consumption in Specifications. 10. Update Figure 23 and note in Power On/Off Sequence. 11. Add Figure 33 in Line Format. 12. Update frequency of SPI_CLK in SPI WRITE. 13. Update Figure 24 in Reset Sequence. 14. Update Figure 28 and note in Trigger and Sensor Line Time.
V0.3.1	09/01/2025	1. Update Features and Specifications. 2. Update Table 6 in Power Consumption. 3. Update note and add Table 8 in Key Specification. 4. Add Figure 11 in Temporal Dark Noise Distribution. 5. Add Table 11 in Register Map. 6. Add Table 22 in Analog Gain. 7. Update table in Product Ordering Information. 8. Add note of Figure 24 in Reset Sequence. 9. Update working mode in Sensor Operation Overview. 10. Update Figure 27 in Clock System. 11. Update note for 10-bit mode of Table 17 in Data Interface Training. 12. Update description of maximal data rate in Channel Multiplexing. 13. Update 10bit description and Figure 31 in Line Format. 14. Update Figure 23 and note in Power On/Off Sequence. 15. Add 10bit setting in Table 20 in SYNC Code. 16. Add 10bit mode in Test Image. 17. Add Figure 40 and update description in Image Flipping. 18. Update Figure 42 in Digital Temperature Sensor. 19. Update note number in Table 7 in Key Specification. 20. Update description in Dark Current with Different Die Temperature. 21. Update description in Spectral Sensitivity Characteristics. 22. Update data name in Figure 12 and Table 9 in Spectral Sensitivity Characteristics.
V0.3.2	23/01/2025	1. Add Test Images, Defect Definitions and Defect Limits in Blemish Specification. 2. Update Figure 2 and note in Package Outline. 3. Update default value in Table 16 in Internal Line Time. 4. Updat Specifications.

		5. Update Table 7, Table 8 and note in Key Specification. 6. Update P1 description and Figure 11 in Temporal Dark Noise Distribution. 7. Update Figure 12, Table 9 and note in Spectral Sensitivity Characteristics. 8. Update Dark Current with Different Die Temperature. 9. Update Table 10 and Table 11 in Register Map. 10. Update note and add Figure 43 in Digital Temperature Sensor. 11. Update table name of Table 6 in Power Consumption. 12. Update frequency of CLK_REF in Clock System. 13. Update Figure 28 and note in Trigger and Sensor Line Time. 14. Update Figure 32 in Line Format. 15. Update Table 30 and description in Blemish Specification. 16. Update Table 33 in Defect Limits.
V0.3.3	25/02/2025	1. Update Figure 31 in Line Format. 2. Update Table 21 and Table 22 and add note in Analog Gain. 3. Update Figure 23 and add Table 13 in Power On/Off Sequence. 4. Update config description and note in Power On/Off Sequence. 5. Update Table 11 in Register Map. 6. Update Figure 19 in Bias Pin Connections. 7. Update Figure 2 in Package Outline. 8. Update Table 1 in Pin Description. 9. Update note in Reset Sequence.
V0.3.4	28/04/2025	1. Correct format of value in Power On/Off Sequence. 2. Update description of bias pins in Table 1 in Pin Description. 3. Update Figure 24 and note in Reset Sequence. 4. Update voltage of V_{OD} in Table 2 in DC Characteristics. 5. Update voltage of Differential output voltage in Table 5 in AC Characteristics. 6. Update Figure 29 in Block Based Readout.
V0.3.5	15/10/2025	1. Update Absolute Maximum Rating. 2. Update Register Map. 3. Update Table 6 and add note. 4. Update Power On/Off Sequence 5. Update Reset Sequence 6. Add Table 19 Minimum sensor line time under each channel output mode. 7. Add Sensor Settling Time. 8. Update Figure 33 and add note in Line Format. 9. Update note in Analog Temperature Diode Connections. 10. Update note in Digital Temperature Sensor. 11. Update description in Analog Temperature Sensor. 12. Update note of Figure 28 in Trigger and Sensor Line Time. 13. Add note in OTP Memory Readout. 14. Add OTP Data Description.

Absolute Maximum Rating

Item	Symbol	Rating	Unit	Remarks
Supply Voltage (Analog 3.3V)	VDDA	-0.3 to 3.63	V	
Supply Voltage (Interface 3.3V)	VDDIO	-0.3 to 3.63	V	
Supply Voltage	VDDD;VDDAD;VDDPLL	-0.3 to 1.67	V	
Supply Voltage (Pixel Voltage)	VDDSF;VDDPIX;VAGH;VBGH; VTXH;VABG;VABGN;VABD; VRSTH;VSELH;VDDPS;VRSTL	-0.3 to 3.63	V	
Supply Voltage (Pixel Voltage)	VAGL;VBGL; VTXL	-2 to 0.3	V	
Input Voltage	VI	-0.3 to VDDIO+0.3	V	NOT exceed 3.63V
Output Voltage	VO	-0.3 to VDDIO+0.3	V	NOT exceed 3.63V
Operation Temperature	Topr	0 ~ 60	℃	Junction temperature
Storage Temperature	Tstg	TBD	℃	Environment temperature

Sensor Operation Overview

GLT5016BSI is designed with two bands. Both P1 and P2 bands have an array of 5μm pixels. The photosensitive area of P1 band is 82.08mm*1.28mm, and P2 band is 82.08mm*0.16mm.

GLT5016BSI supports two working modes:

12-bit ADC single band mode: P1 band with 5μm pixel size.

10-bit ADC single band mode: P1 band with 5μm pixel size.

The minimum pixel size of two bands is 5μm x 5μm. The pixels are readout from the bottom readout chain, pixel readouts are shown in Figure 1.

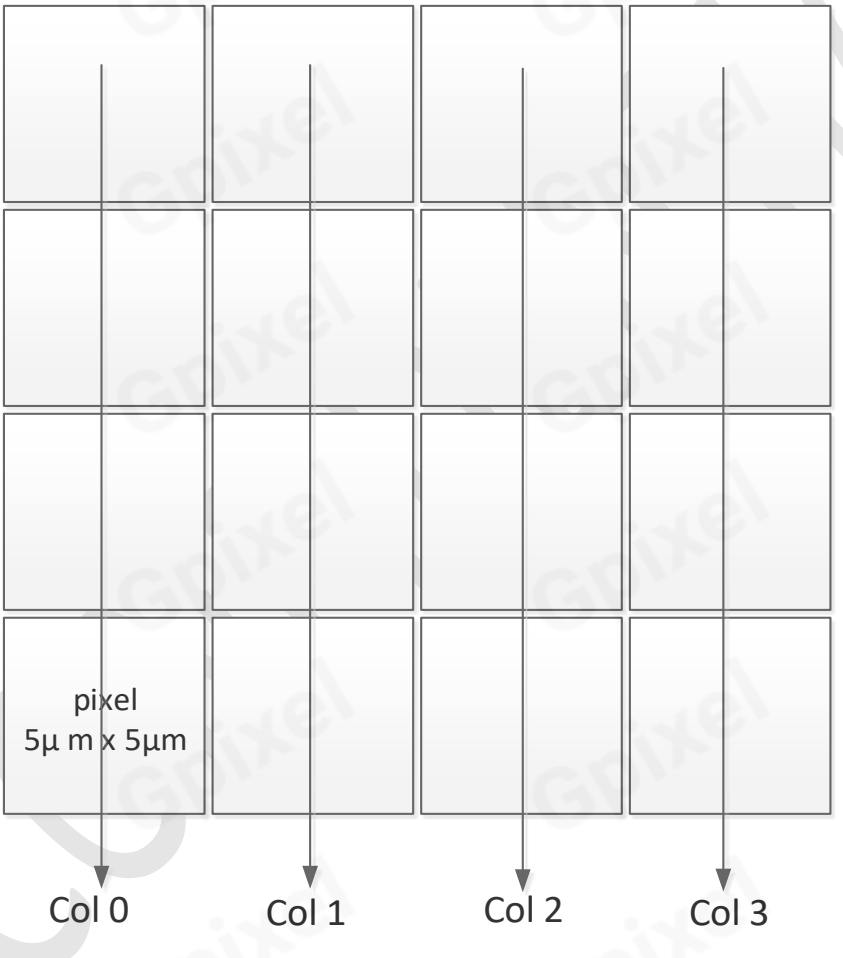


Figure 1 Pixel readout

NOTE:

1) For use of dual band mode, please contact Gpixel.

CONTENT

Package Outline

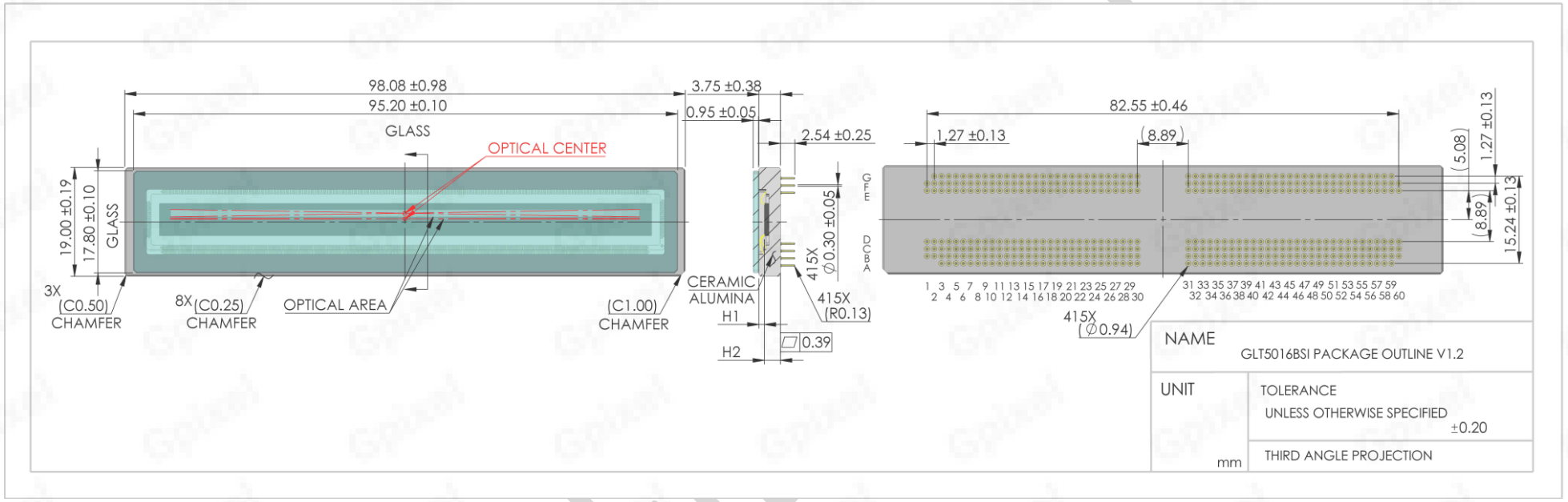


Figure 2 Package outline

NOTE:

1) The centers of the optical sensitive area (OPTICAL CENTER) relative to lower-left of ceramic package outline are:
   (X , Y) = (49.040 , 11.013) ± 0.20mm for P1 (top area);
   (X , Y) = (49.040 , 10.033) ± 0.20mm for P2 (lower area).
2) The rotation angle of the die relative to ceramic package outline is ± 0.3°. The tilt of the die relative to die attach surface of the ceramic package is less than 0.2 mm.
3) The height from the die surface to the top of the ceramic package is 0.95 ± 0.405 mm (H1).
4) The height from the die surface to the bottom of the ceramic package (exclude the pin height) is 2.8 ± 0.255 mm (H2).
5) The thermal conductivity of the ceramic package is 18 W/(mK).
6) The thermal expansion coefficient of the ceramic package is 7.6 x 10^{-6}/K from room temperature (25 ± 5°C) to 800°C.

Optical Center & Temperature Sensor

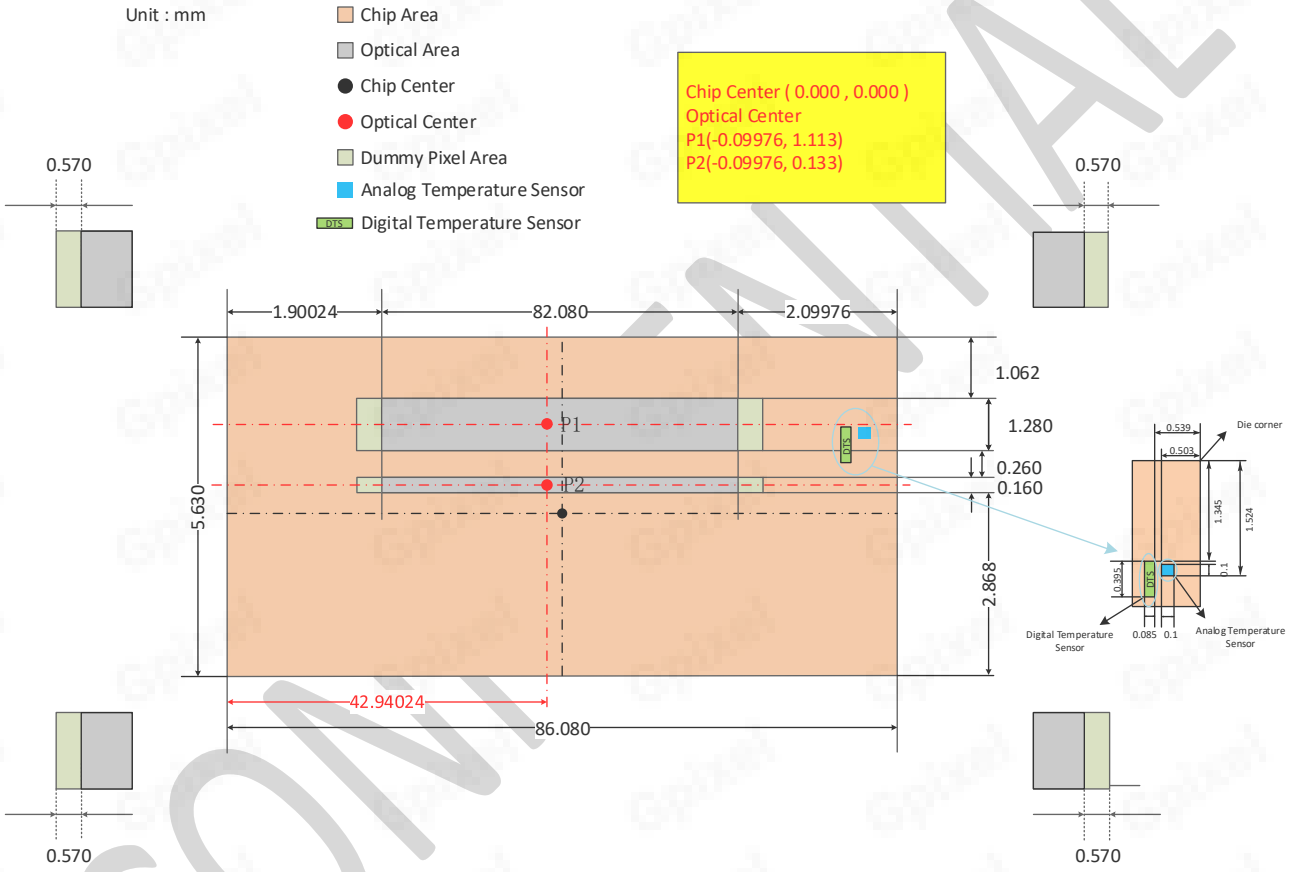
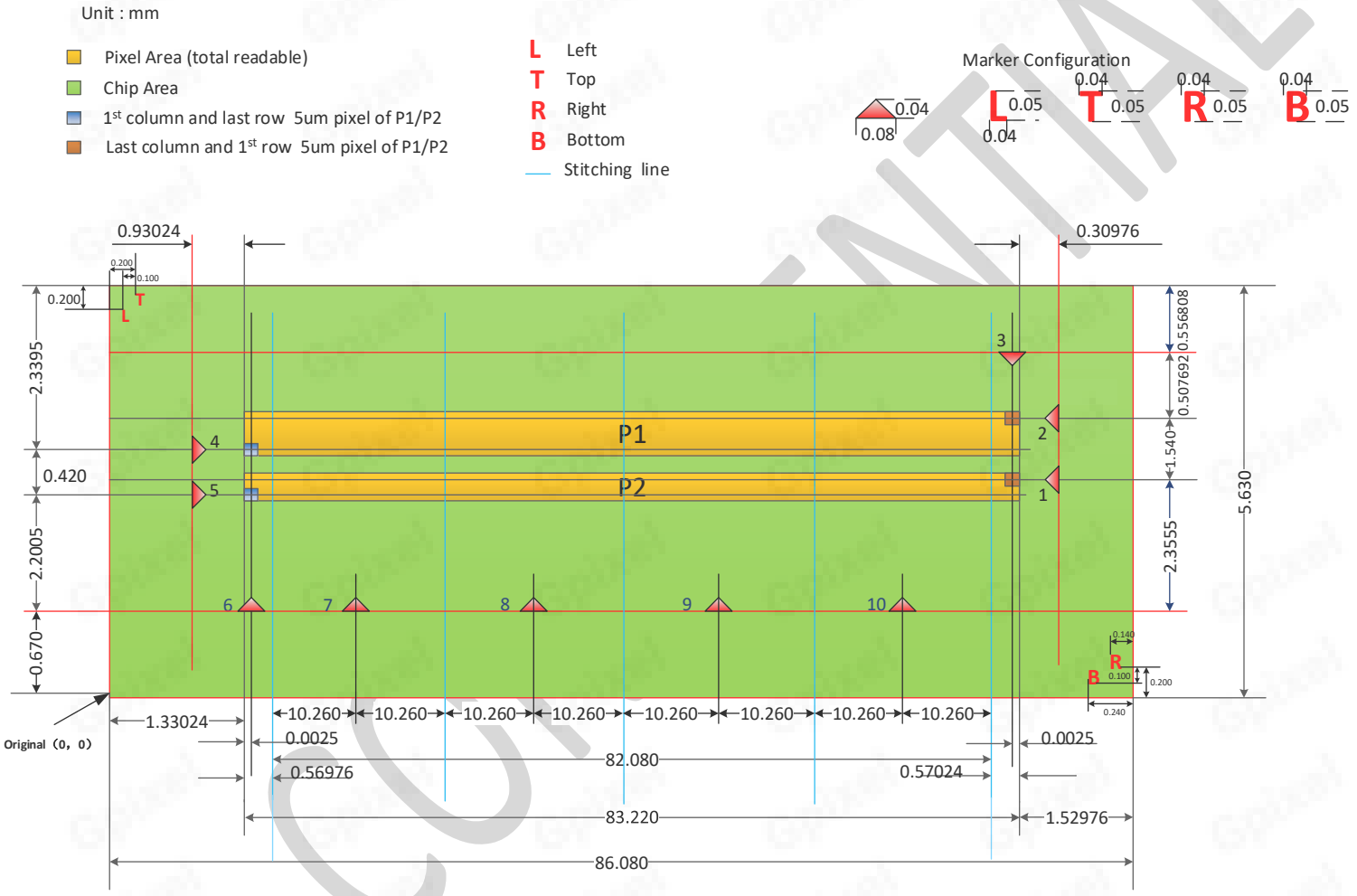


Figure 3 Optical center

NOTE:

1) Optical center is with reference to Chip (silicon die) center, for camera mechanic design, please refer to package outline for optical center with reference to sensor package in Figure 2.

Optical Marker



Marker right-angled vertex coordinate:

Marker1	(84.820,3.0255)
Marker2	(84.820,4.5655)
Marker3	(84.54774,5.033192)
Marker4	(0.440,3.2905)
Marker5	(0.440,2.8705)
Marker6	(1.33274,0.710)
Marker7	(12.160,0.710)
Marker8	(32.680,0.710)
Marker9	(53.200,0.710)
Marker10	(73.720,0.710)

Figure 4 GLT5016BSI optical marker

Pixel Arrangement

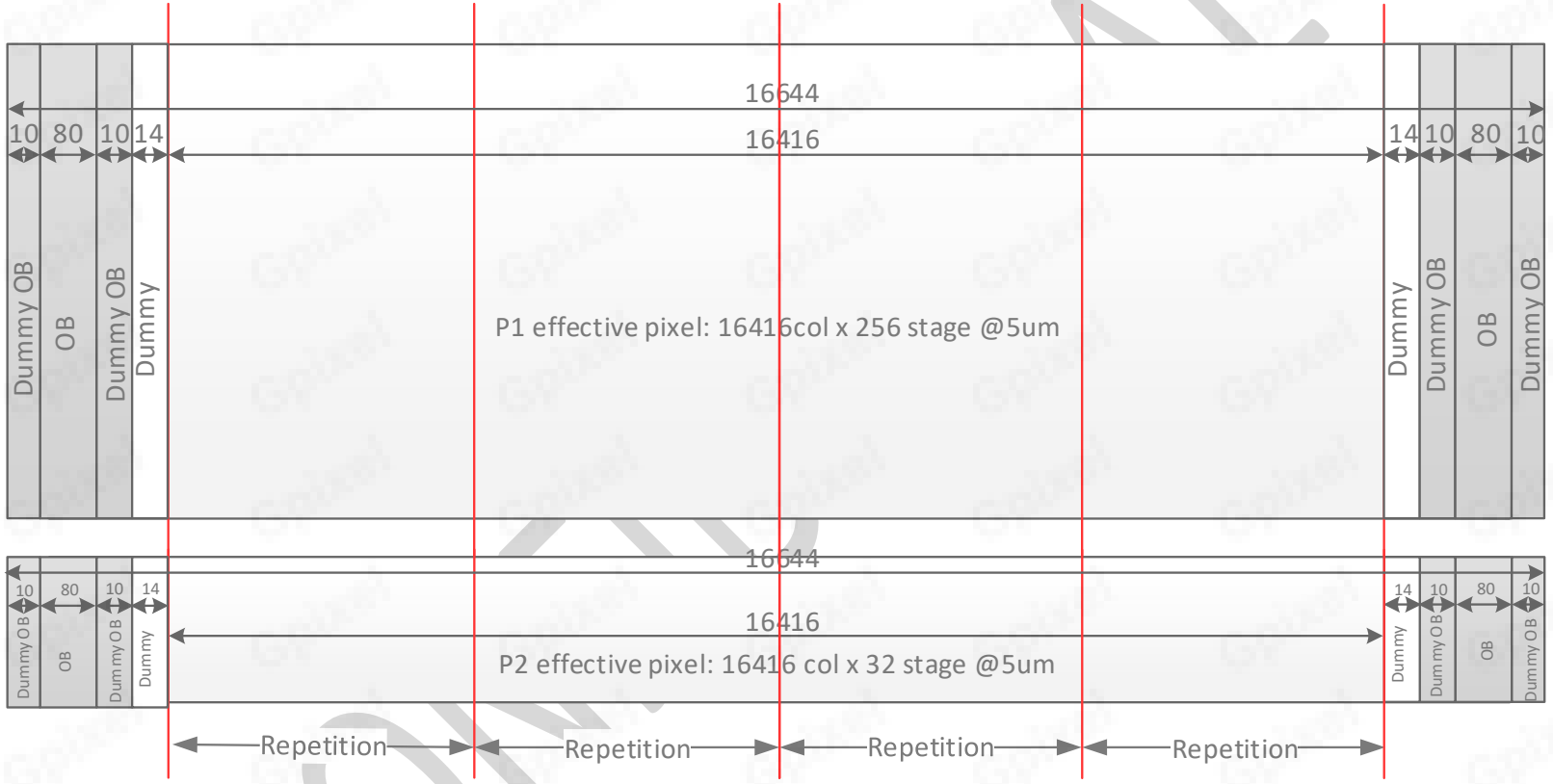


Figure 5 Pixel arrangement

Internal Block Diagram and Pin Configuration

Internal Block Diagram

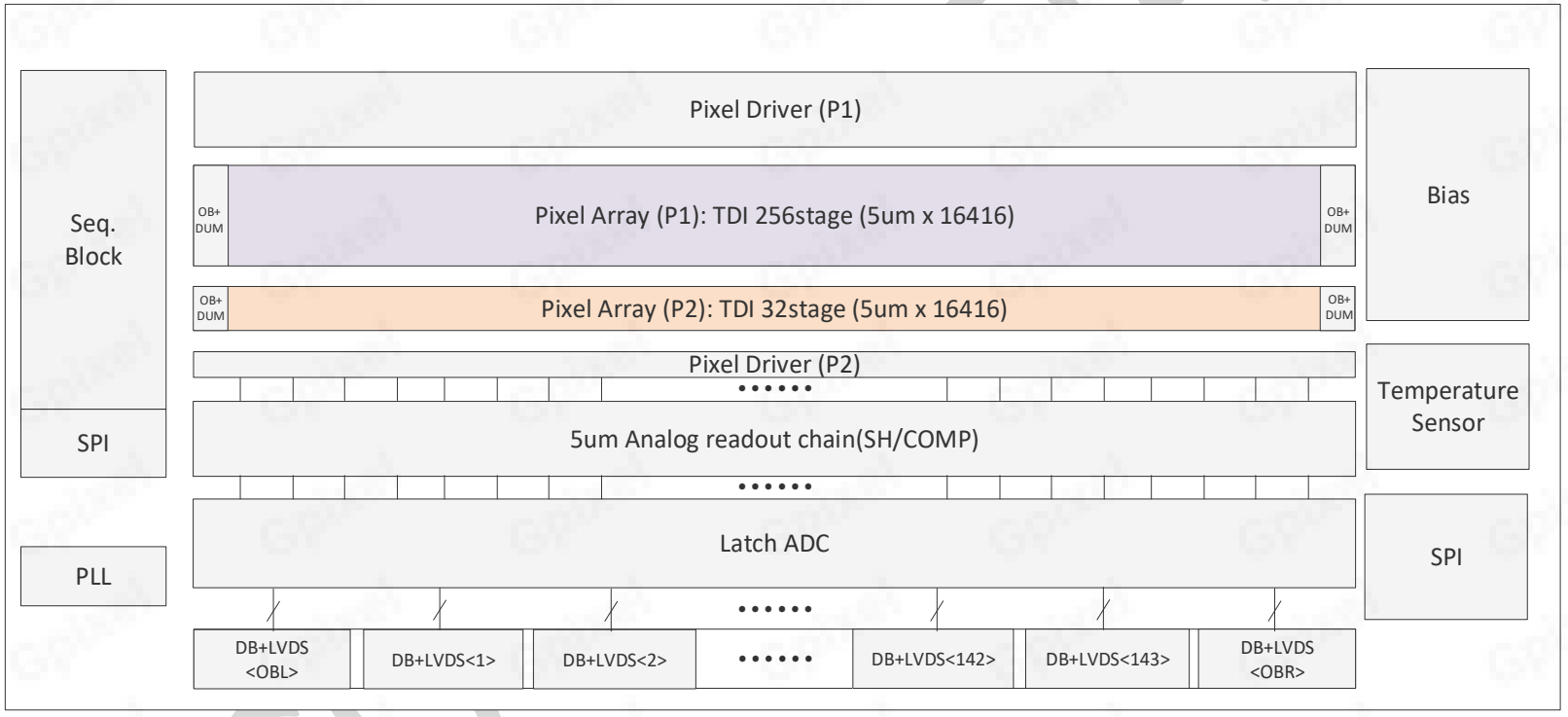


Figure 6 Block diagram

Pin Description

Table 1 Pin description

NO.	Pin No.	I/O	Symbol	Description	Type
1	A3	GND	PSUB	Pixel ground	Ground
2	A4	I/O	VDP	Analog temperature sensor positive node	Analog input/output
3	A5	I/O	VDN	Analog temperature sensor negative node	Analog input/output
4	A6	-	NC	N/A	Leave floating
5	A7	O	DDR_N<3>	Sub-LVDS clock negative output 3	Sub-LVDS output
6	A8	POWER	VDDD	Digital supply	Supply
7	A9	O	LVDS_N<143>	Sub-LVDS data negative channel 143	Sub-LVDS output
8	A10	O	LVDS_N<123>	Sub-LVDS data negative channel 123	Sub-LVDS output
9	A11	POWER	VDDAD	Digital supply	Supply
10	A12	POWER	VDDD	Digital supply	Supply
11	A13	POWER	VDDA	Analog supply	Supply
12	A14	-	NC	N/A	Leave floating
13	A15	O	DDR_N<2>	Sub-LVDS clock negative output 2	Sub-LVDS output
14	A16	POWER	VDDD	Digital supply	Supply
15	A17	POWER	VDDAD	Digital supply	Supply
16	A18	O	LVDS_N<114>	Sub-LVDS data negative channel 114	Sub-LVDS output
17	A19	-	NC	N/A	Leave floating
18	A20	-	NC	N/A	Leave floating
19	A21	O	LVDS_N<91>	Sub-LVDS data negative channel 91	Sub-LVDS output
20	A22	O	LVDS_N<83>	Sub-LVDS data negative channel 83	Sub-LVDS output
21	A23	POWER	VDDA	Analog supply	Supply
22	A24	O	LVDS_N<78>	Sub-LVDS data negative channel 78	Sub-LVDS output
23	A25	O	LVDS_N<74>	Sub-LVDS data negative channel 74	Sub-LVDS output
24	A26	POWER	VDDD	Digital supply	Supply
25	A27	O	LVDS_N<73>	Sub-LVDS data negative channel 73	Sub-LVDS output
26	A28	POWER	VDDAD	Digital supply	Supply
27	A29	O	LVDS_N<75>	Sub-LVDS data negative channel 75	Sub-LVDS output
28	A30	-	NC	N/A	Leave floating
29	A31	O	LVDS_N<70>	Sub-LVDS data negative channel 70	Sub-LVDS output
30	A32	O	LVDS_N<71>	Sub-LVDS data negative channel 71	Sub-LVDS output
31	A33	O	DDR_N<1>	Sub-LVDS clock negative output 1	Sub-LVDS output
32	A34	POWER	VDDD	Digital supply	Supply
33	A35	-	NC	N/A	Leave floating
34	A36	O	LVDS_N<65>	Sub-LVDS data negative channel 65	Sub-LVDS output
35	A37	-	NC	N/A	Leave floating
36	A38	-	NC	N/A	Leave floating

37	A39	POWER	VDDAD	Digital supply	Supply
38	A40	POWER	VDDD	Digital supply	Supply
39	A41	POWER	VDDA	Analog supply	Supply
40	A42	-	NC	N/A	Leave floating
41	A43	O	DDR_N<0>	Sub-LVDS clock negative output 0	Sub-LVDS output
42	A44	O	LVDS_N<49>	Sub-LVDS data negative channel 49	Sub-LVDS output
43	A45	POWER	VDDAD	Digital supply	Supply
44	A46	POWER	VDDD	Digital supply	Supply
45	A47	O	LVDS_N<9>	Sub-LVDS data negative channel 9	Sub-LVDS output
46	A48	-	NC	N/A	Leave floating
47	A49	O	LVDS_N<13>	Sub-LVDS data negative channel 13	Sub-LVDS output
48	A50	-	NC	N/A	Leave floating
49	A51	POWER	VDDA	Analog supply	Supply
50	A52	POWER	VDDAD	Digital supply	Supply
51	A53	POWER	VDDD	Digital supply	Supply
52	A54	O	LVDS_N<2>	Sub-LVDS data negative channel 2	Sub-LVDS output
53	A55	POWER	VDDPLL	Analog supply	Supply
54	A56	GND	PSUB	Pixel ground	Ground
55	A57	I	TRIG	External trigger	Digital input
56	A58	O	SPI_OUT	SPI output	Digital output
57	A59	I	CLK_REF	PLL reference clock	Digital input
58	B1	-	NC	N/A	Leave floating
59	B2	POWER	VDDPS	Pixel supply	Supply
60	B3	I/O	VBG	On-chip generated bias voltage	Bias
61	B4	O	TANA	Analog test pin	Analog test
62	B5	O	AG_TEST	Analog test pin	Analog test
63	B6	-	NC	N/A	Leave floating
64	B7	O	DDR_P<3>	Sub-LVDS clock positive output 3	Sub-LVDS output
65	B8	GND	GNDD	Ground	Ground
66	B9	O	LVDS_P<143>	Sub-LVDS data positive channel 143	Sub-LVDS output
67	B10	O	LVDS_P<123>	Sub-LVDS data positive channel 123	Sub-LVDS output
68	B11	GND	GNDAD	Ground	Ground
69	B12	GND	GNDD	Ground	Ground
70	B13	GND	GNDA	Ground	Ground
71	B14	-	NC	N/A	Leave floating
72	B15	O	DDR_P<2>	Sub-LVDS clock positive output 2	Sub-LVDS output
73	B16	GND	GNDD	Ground	Ground
74	B17	GND	GNDAD	Ground	Ground
75	B18	O	LVDS_P<114>	Sub-LVDS data positive channel 114	Sub-LVDS output
76	B19	-	NC	N/A	Leave floating
77	B20	-	NC	N/A	Leave floating
78	B21	O	LVDS_P<91>	Sub-LVDS data positive channel 91	Sub-LVDS output

79	B22	O	LVDS_P<83>	Sub-LVDS data positive channel 83	Sub-LVDS output
80	B23	GND	GNDA	Ground	Ground
81	B24	O	LVDS_P<78>	Sub-LVDS data positive channel 78	Sub-LVDS output
82	B25	O	LVDS_P<74>	Sub-LVDS data positive channel 74	Sub-LVDS output
83	B26	GND	GNDD	Ground	Ground
84	B27	O	LVDS_P<73>	Sub-LVDS data positive channel 73	Sub-LVDS output
85	B28	GND	GNDAD	Ground	Ground
86	B29	O	LVDS_P<75>	Sub-LVDS data positive channel 75	Sub-LVDS output
87	B30	-	NC	N/A	Leave floating
88	B31	O	LVDS_P<70>	Sub-LVDS data positive channel 70	Sub-LVDS output
89	B32	O	LVDS_P<71>	Sub-LVDS data positive channel 71	Sub-LVDS output
90	B33	O	DDR_P<1>	Sub-LVDS clock positive output 1	Sub-LVDS output
91	B34	GND	GNDD	Ground	Ground
92	B35	-	NC	N/A	Leave floating
93	B36	O	LVDS_P<65>	Sub-LVDS data positive channel 65	Sub-LVDS output
94	B37	-	NC	N/A	Leave floating
95	B38	-	NC	N/A	Leave floating
96	B39	GND	GNDAD	Ground	Ground
97	B40	GND	GNDD	Ground	Ground
98	B41	GND	GNDA	Ground	Ground
99	B42	-	NC	N/A	Leave floating
100	B43	O	DDR_P<0>	Sub-LVDS clock positive output 0	Sub-LVDS output
101	B44	O	LVDS_P<49>	Sub-LVDS data positive channel 49	Sub-LVDS output
102	B45	GND	GNDAD	Ground	Ground
103	B46	GND	GNDD	Ground	Ground
104	B47	O	LVDS_P<9>	Sub-LVDS data positive channel 9	Sub-LVDS output
105	B48	-	NC	N/A	Leave floating
106	B49	O	LVDS_P<13>	Sub-LVDS data positive channel 13	Sub-LVDS output
107	B50	-	NC	N/A	Leave floating
108	B51	GND	GNDA	Ground	Ground
109	B52	GND	GNDAD	Ground	Ground
110	B53	GND	GNDD	Ground	Ground
111	B54	O	LVDS_P<2>	Sub-LVDS data positive channel 2	Sub-LVDS output
112	B55	GND	GNDPLL	Ground	Ground
113	B56	POWER	VDDIO	IO ring supply	Supply
114	B57	I	SPI_CS_N	SPI input	Digital input
115	B58	I	SYS_RST_N	System reset signal	Digital input
116	B59	I	SPI_IN	SPI input	Digital input
117	B60	I	SPI_CLK	SPI clock	Digital input
118	C1	O	LVDS_N<141>	Sub-LVDS data negative channel 141	Sub-LVDS output
119	C2	O	LVDS_N<139>	Sub-LVDS data negative channel 139	Sub-LVDS output
120	C3	O	LVDS_N<137>	Sub-LVDS data negative channel 137	Sub-LVDS output

121	C4	O	LVDS_N<135>	Sub-LVDS data negative channel 135	Sub-LVDS output
122	C5	O	LVDS_N<133>	Sub-LVDS data negative channel 133	Sub-LVDS output
123	C6	O	LVDS_N<130>	Sub-LVDS data negative channel 130	Sub-LVDS output
124	C7	-	NC	N/A	Leave floating
125	C8	O	LVDS_N<126>	Sub-LVDS data negative channel 126	Sub-LVDS output
126	C9	-	NC	N/A	Leave floating
127	C10	O	LVDS_N<121>	Sub-LVDS data negative channel 121	Sub-LVDS output
128	C11	O	LVDS_N<119>	Sub-LVDS data negative channel 119	Sub-LVDS output
129	C12	O	LVDS_N<117>	Sub-LVDS data negative channel 117	Sub-LVDS output
130	C13	O	LVDS_N<115>	Sub-LVDS data negative channel 115	Sub-LVDS output
131	C14	-	NC	N/A	Leave floating
132	C15	O	LVDS_N<110>	Sub-LVDS data negative channel 110	Sub-LVDS output
133	C16	-	NC	N/A	Leave floating
134	C17	O	LVDS_N<106>	Sub-LVDS data negative channel 106	Sub-LVDS output
135	C18	O	LVDS_N<103>	Sub-LVDS data negative channel 103	Sub-LVDS output
136	C19	O	LVDS_N<102>	Sub-LVDS data negative channel 102	Sub-LVDS output
137	C20	O	LVDS_N<99>	Sub-LVDS data negative channel 99	Sub-LVDS output
138	C21	O	LVDS_N<97>	Sub-LVDS data negative channel 97	Sub-LVDS output
139	C22	O	LVDS_N<95>	Sub-LVDS data negative channel 95	Sub-LVDS output
140	C23	O	LVDS_N<93>	Sub-LVDS data negative channel 93	Sub-LVDS output
141	C24	O	LVDS_N<90>	Sub-LVDS data negative channel 90	Sub-LVDS output
142	C25	-	NC	N/A	Leave floating
143	C26	O	LVDS_N<86>	Sub-LVDS data negative channel 86	Sub-LVDS output
144	C27	-	NC	N/A	Leave floating
145	C28	O	LVDS_N<81>	Sub-LVDS data negative channel 81	Sub-LVDS output
146	C29	O	LVDS_N<79>	Sub-LVDS data negative channel 79	Sub-LVDS output
147	C30	O	LVDS_N<77>	Sub-LVDS data negative channel 77	Sub-LVDS output
148	C31	O	LVDS_N<69>	Sub-LVDS data negative channel 69	Sub-LVDS output
149	C32	O	LVDS_N<67>	Sub-LVDS data negative channel 67	Sub-LVDS output
150	C33	-	NC	N/A	Leave floating
151	C34	O	LVDS_N<62>	Sub-LVDS data negative channel 62	Sub-LVDS output
152	C35	O	LVDS_N<59>	Sub-LVDS data negative channel 59	Sub-LVDS output
153	C36	O	LVDS_N<57>	Sub-LVDS data negative channel 57	Sub-LVDS output
154	C37	O	LVDS_N<55>	Sub-LVDS data negative channel 55	Sub-LVDS output
155	C38	O	LVDS_N<53>	Sub-LVDS data negative channel 53	Sub-LVDS output
156	C39	O	LVDS_N<51>	Sub-LVDS data negative channel 51	Sub-LVDS output
157	C40	-	NC	N/A	Leave floating
158	C41	O	LVDS_N<46>	Sub-LVDS data negative channel 46	Sub-LVDS output
159	C42	-	NC	N/A	Leave floating
160	C43	O	LVDS_N<42>	Sub-LVDS data negative channel 42	Sub-LVDS output
161	C44	O	LVDS_N<39>	Sub-LVDS data negative channel 39	Sub-LVDS output
162	C45	O	LVDS_N<37>	Sub-LVDS data negative channel 37	Sub-LVDS output

163	C46	O	LVDS_N<34>	Sub-LVDS data negative channel 34	Sub-LVDS output
164	C47	O	LVDS_N<33>	Sub-LVDS data negative channel 33	Sub-LVDS output
165	C48	O	LVDS_N<30>	Sub-LVDS data negative channel 30	Sub-LVDS output
166	C49	-	NC	N/A	Leave floating
167	C50	O	LVDS_N<26>	Sub-LVDS data negative channel 26	Sub-LVDS output
168	C51	O	LVDS_N<23>	Sub-LVDS data negative channel 23	Sub-LVDS output
169	C52	O	LVDS_N<21>	Sub-LVDS data negative channel 21	Sub-LVDS output
170	C53	O	LVDS_N<19>	Sub-LVDS data negative channel 19	Sub-LVDS output
171	C54	O	LVDS_N<17>	Sub-LVDS data negative channel 17	Sub-LVDS output
172	C55	O	LVDS_N<15>	Sub-LVDS data negative channel 15	Sub-LVDS output
173	C56	-	NC	N/A	Leave floating
174	C57	O	LVDS_N<10>	Sub-LVDS data negative channel 10	Sub-LVDS output
175	C58	-	NC	N/A	Leave floating
176	C59	O	LVDS_N<6>	Sub-LVDS data negative channel 6	Sub-LVDS output
177	C60	-	NC	N/A	Leave floating
178	D1	O	LVDS_P<141>	Sub-LVDS data positive channel 141	Sub-LVDS output
179	D2	O	LVDS_P<139>	Sub-LVDS data positive channel 139	Sub-LVDS output
180	D3	O	LVDS_P<137>	Sub-LVDS data positive channel 137	Sub-LVDS output
181	D4	O	LVDS_P<135>	Sub-LVDS data positive channel 135	Sub-LVDS output
182	D5	O	LVDS_P<133>	Sub-LVDS data positive channel 133	Sub-LVDS output
183	D6	O	LVDS_P<130>	Sub-LVDS data positive channel 130	Sub-LVDS output
184	D7	-	NC	N/A	Leave floating
185	D8	O	LVDS_P<126>	Sub-LVDS data positive channel 126	Sub-LVDS output
186	D9	-	NC	N/A	Leave floating
187	D10	O	LVDS_P<121>	Sub-LVDS data positive channel 121	Sub-LVDS output
188	D11	O	LVDS_P<119>	Sub-LVDS data positive channel 119	Sub-LVDS output
189	D12	O	LVDS_P<117>	Sub-LVDS data positive channel 117	Sub-LVDS output
190	D13	O	LVDS_P<115>	Sub-LVDS data positive channel 115	Sub-LVDS output
191	D14	-	NC	N/A	Leave floating
192	D15	O	LVDS_P<110>	Sub-LVDS data positive channel 110	Sub-LVDS output
193	D16	-	NC	N/A	Leave floating
194	D17	O	LVDS_P<106>	Sub-LVDS data positive channel 106	Sub-LVDS output
195	D18	O	LVDS_P<103>	Sub-LVDS data positive channel 103	Sub-LVDS output
196	D19	O	LVDS_P<102>	Sub-LVDS data positive channel 102	Sub-LVDS output
197	D20	O	LVDS_P<99>	Sub-LVDS data positive channel 99	Sub-LVDS output
198	D21	O	LVDS_P<97>	Sub-LVDS data positive channel 97	Sub-LVDS output
199	D22	O	LVDS_P<95>	Sub-LVDS data positive channel 95	Sub-LVDS output
200	D23	O	LVDS_P<93>	Sub-LVDS data positive channel 93	Sub-LVDS output
201	D24	O	LVDS_P<90>	Sub-LVDS data positive channel 90	Sub-LVDS output
202	D25	-	NC	N/A	Leave floating
203	D26	O	LVDS_P<86>	Sub-LVDS data positive channel 86	Sub-LVDS output
204	D27	-	NC	N/A	Leave floating

205	D28	O	LVDS_P<81>	Sub-LVDS data positive channel 81	Sub-LVDS output
206	D29	O	LVDS_P<79>	Sub-LVDS data positive channel 79	Sub-LVDS output
207	D30	O	LVDS_P<77>	Sub-LVDS data positive channel 77	Sub-LVDS output
208	D31	O	LVDS_P<69>	Sub-LVDS data positive channel 69	Sub-LVDS output
209	D32	O	LVDS_P<67>	Sub-LVDS data positive channel 67	Sub-LVDS output
210	D33	-	NC	N/A	Leave floating
211	D34	O	LVDS_P<62>	Sub-LVDS data positive channel 62	Sub-LVDS output
212	D35	O	LVDS_P<59>	Sub-LVDS data positive channel 59	Sub-LVDS output
213	D36	O	LVDS_P<57>	Sub-LVDS data positive channel 57	Sub-LVDS output
214	D37	O	LVDS_P<55>	Sub-LVDS data positive channel 55	Sub-LVDS output
215	D38	O	LVDS_P<53>	Sub-LVDS data positive channel 53	Sub-LVDS output
216	D39	O	LVDS_P<51>	Sub-LVDS data positive channel 51	Sub-LVDS output
217	D40	-	NC	N/A	Leave floating
218	D41	O	LVDS_P<46>	Sub-LVDS data positive channel 46	Sub-LVDS output
219	D42	-	NC	N/A	Leave floating
220	D43	O	LVDS_P<42>	Sub-LVDS data positive channel 42	Sub-LVDS output
221	D44	O	LVDS_P<39>	Sub-LVDS data positive channel 39	Sub-LVDS output
222	D45	O	LVDS_P<37>	Sub-LVDS data positive channel 37	Sub-LVDS output
223	D46	O	LVDS_P<34>	Sub-LVDS data positive channel 34	Sub-LVDS output
224	D47	O	LVDS_P<33>	Sub-LVDS data positive channel 33	Sub-LVDS output
225	D48	O	LVDS_P<30>	Sub-LVDS data positive channel 30	Sub-LVDS output
226	D49	-	NC	N/A	Leave floating
227	D50	O	LVDS_P<26>	Sub-LVDS data positive channel 26	Sub-LVDS output
228	D51	O	LVDS_P<23>	Sub-LVDS data positive channel 23	Sub-LVDS output
229	D52	O	LVDS_P<21>	Sub-LVDS data positive channel 21	Sub-LVDS output
230	D53	O	LVDS_P<19>	Sub-LVDS data positive channel 19	Sub-LVDS output
231	D54	O	LVDS_P<17>	Sub-LVDS data positive channel 17	Sub-LVDS output
232	D55	O	LVDS_P<15>	Sub-LVDS data positive channel 15	Sub-LVDS output
233	D56	-	NC	N/A	Leave floating
234	D57	O	LVDS_P<10>	Sub-LVDS data positive channel 10	Sub-LVDS output
235	D58	-	NC	N/A	Leave floating
236	D59	O	LVDS_P<6>	Sub-LVDS data positive channel 6	Sub-LVDS output
237	D60	-	NC	N/A	Leave floating
238	E1	I/O	VLBN	On-chip generated bias voltage	Bias
239	E2	O	LVDS_N<145>	Sub-LVDS data negative channel 145	Sub-LVDS output
240	E3	O	LVDS_N<142>	Sub-LVDS data negative channel 142	Sub-LVDS output
241	E4	-	NC	N/A	Leave floating
242	E5	O	LVDS_N<138>	Sub-LVDS data negative channel 138	Sub-LVDS output
243	E6	-	NC	N/A	Leave floating
244	E7	O	LVDS_N<134>	Sub-LVDS data negative channel 134	Sub-LVDS output
245	E8	O	LVDS_N<131>	Sub-LVDS data negative channel 131	Sub-LVDS output
246	E9	O	LVDS_N<129>	Sub-LVDS data negative channel 129	Sub-LVDS output

247	E10	O	LVDS_N<127>	Sub-LVDS data negative channel 127	Sub-LVDS output
248	E11	O	LVDS_N<125>	Sub-LVDS data negative channel 125	Sub-LVDS output
249	E12	O	LVDS_N<122>	Sub-LVDS data negative channel 122	Sub-LVDS output
250	E13	-	NC	N/A	Leave floating
251	E14	O	LVDS_N<118>	Sub-LVDS data negative channel 118	Sub-LVDS output
252	E15	-	NC	N/A	Leave floating
253	E16	O	LVDS_N<113>	Sub-LVDS data negative channel 113	Sub-LVDS output
254	E17	O	LVDS_N<111>	Sub-LVDS data negative channel 111	Sub-LVDS output
255	E18	O	LVDS_N<109>	Sub-LVDS data negative channel 109	Sub-LVDS output
256	E19	O	LVDS_N<107>	Sub-LVDS data negative channel 107	Sub-LVDS output
257	E20	O	LVDS_N<105>	Sub-LVDS data negative channel 105	Sub-LVDS output
258	E21	O	LVDS_N<101>	Sub-LVDS data negative channel 101	Sub-LVDS output
259	E22	O	LVDS_N<98>	Sub-LVDS data negative channel 98	Sub-LVDS output
260	E23	-	NC	N/A	Leave floating
261	E24	O	LVDS_N<94>	Sub-LVDS data negative channel 94	Sub-LVDS output
262	E25	-	NC	N/A	Leave floating
263	E26	O	LVDS_N<89>	Sub-LVDS data negative channel 89	Sub-LVDS output
264	E27	O	LVDS_N<87>	Sub-LVDS data negative channel 87	Sub-LVDS output
265	E28	O	LVDS_N<85>	Sub-LVDS data negative channel 85	Sub-LVDS output
266	E29	O	LVDS_N<82>	Sub-LVDS data negative channel 82	Sub-LVDS output
267	E30	-	NC	N/A	Leave floating
268	E31	O	LVDS_N<66>	Sub-LVDS data negative channel 66	Sub-LVDS output
269	E32	O	LVDS_N<63>	Sub-LVDS data negative channel 63	Sub-LVDS output
270	E33	O	LVDS_N<61>	Sub-LVDS data negative channel 61	Sub-LVDS output
271	E34	O	LVDS_N<58>	Sub-LVDS data negative channel 58	Sub-LVDS output
272	E35	-	NC	N/A	Leave floating
273	E36	O	LVDS_N<54>	Sub-LVDS data negative channel 54	Sub-LVDS output
274	E37	-	NC	N/A	Leave floating
275	E38	O	LVDS_N<50>	Sub-LVDS data negative channel 50	Sub-LVDS output
276	E39	O	LVDS_N<47>	Sub-LVDS data negative channel 47	Sub-LVDS output
277	E40	O	LVDS_N<45>	Sub-LVDS data negative channel 45	Sub-LVDS output
278	E41	O	LVDS_N<43>	Sub-LVDS data negative channel 43	Sub-LVDS output
279	E42	O	LVDS_N<41>	Sub-LVDS data negative channel 41	Sub-LVDS output
280	E43	O	LVDS_N<38>	Sub-LVDS data negative channel 38	Sub-LVDS output
281	E44	O	LVDS_N<35>	Sub-LVDS data negative channel 35	Sub-LVDS output
282	E45	-	NC	N/A	Leave floating
283	E46	O	LVDS_N<31>	Sub-LVDS data negative channel 31	Sub-LVDS output
284	E47	O	LVDS_N<29>	Sub-LVDS data negative channel 29	Sub-LVDS output
285	E48	O	LVDS_N<27>	Sub-LVDS data negative channel 27	Sub-LVDS output
286	E49	O	LVDS_N<25>	Sub-LVDS data negative channel 25	Sub-LVDS output
287	E50	O	LVDS_N<22>	Sub-LVDS data negative channel 22	Sub-LVDS output
288	E51	-	NC	N/A	Leave floating

289	E52	O	LVDS_N<18>	Sub-LVDS data negative channel 18	Sub-LVDS output
290	E53	-	NC	N/A	Leave floating
291	E54	O	LVDS_N<14>	Sub-LVDS data negative channel 14	Sub-LVDS output
292	E55	O	LVDS_N<11>	Sub-LVDS data negative channel 11	Sub-LVDS output
293	E56	O	LVDS_N<7>	Sub-LVDS data negative channel 7	Sub-LVDS output
294	E57	O	LVDS_N<5>	Sub-LVDS data negative channel 5	Sub-LVDS output
295	E58	O	LVDS_N<3>	Sub-LVDS data negative channel 3	Sub-LVDS output
296	E59	O	LVDS_N<1>	Sub-LVDS data negative channel 1	Sub-LVDS output
297	E60	O	LVDS_N<0>	Sub-LVDS data negative channel 0	Sub-LVDS output
298	F1	I/O	VSBP	On-chip generated bias voltage	Bias
299	F2	O	LVDS_P<145>	Sub-LVDS data positive channel 145	Sub-LVDS output
300	F3	O	LVDS_P<142>	Sub-LVDS data positive channel 142	Sub-LVDS output
301	F4	-	NC	N/A	Leave floating
302	F5	O	LVDS_P<138>	Sub-LVDS data positive channel 138	Sub-LVDS output
303	F6	-	NC	N/A	Leave floating
304	F7	O	LVDS_P<134>	Sub-LVDS data positive channel 134	Sub-LVDS output
305	F8	O	LVDS_P<131>	Sub-LVDS data positive channel 131	Sub-LVDS output
306	F9	O	LVDS_P<129>	Sub-LVDS data positive channel 129	Sub-LVDS output
307	F10	O	LVDS_P<127>	Sub-LVDS data positive channel 127	Sub-LVDS output
308	F11	O	LVDS_P<125>	Sub-LVDS data positive channel 125	Sub-LVDS output
309	F12	O	LVDS_P<122>	Sub-LVDS data positive channel 122	Sub-LVDS output
310	F13	-	NC	N/A	Leave floating
311	F14	O	LVDS_P<118>	Sub-LVDS data positive channel 118	Sub-LVDS output
312	F15	-	NC	N/A	Leave floating
313	F16	O	LVDS_P<113>	Sub-LVDS data positive channel 113	Sub-LVDS output
314	F17	O	LVDS_P<111>	Sub-LVDS data positive channel 111	Sub-LVDS output
315	F18	O	LVDS_P<109>	Sub-LVDS data positive channel 109	Sub-LVDS output
316	F19	O	LVDS_P<107>	Sub-LVDS data positive channel 107	Sub-LVDS output
317	F20	O	LVDS_P<105>	Sub-LVDS data positive channel 105	Sub-LVDS output
318	F21	O	LVDS_P<101>	Sub-LVDS data positive channel 101	Sub-LVDS output
319	F22	O	LVDS_P<98>	Sub-LVDS data positive channel 98	Sub-LVDS output
320	F23	-	NC	N/A	Leave floating
321	F24	O	LVDS_P<94>	Sub-LVDS data positive channel 94	Sub-LVDS output
322	F25	-	NC	N/A	Leave floating
323	F26	O	LVDS_P<89>	Sub-LVDS data positive channel 89	Sub-LVDS output
324	F27	O	LVDS_P<87>	Sub-LVDS data positive channel 87	Sub-LVDS output
325	F28	O	LVDS_P<85>	Sub-LVDS data positive channel 85	Sub-LVDS output
326	F29	O	LVDS_P<82>	Sub-LVDS data positive channel 82	Sub-LVDS output
327	F30	-	NC	N/A	Leave floating
328	F31	O	LVDS_P<66>	Sub-LVDS data positive channel 66	Sub-LVDS output
329	F32	O	LVDS_P<63>	Sub-LVDS data positive channel 63	Sub-LVDS output
330	F33	O	LVDS_P<61>	Sub-LVDS data positive channel 61	Sub-LVDS output

331	F34	O	LVDS_P<58>	Sub-LVDS data positive channel 58	Sub-LVDS output
332	F35	-	NC	N/A	Leave floating
333	F36	O	LVDS_P<54>	Sub-LVDS data positive channel 54	Sub-LVDS output
334	F37	-	NC	N/A	Leave floating
335	F38	O	LVDS_P<50>	Sub-LVDS data positive channel 50	Sub-LVDS output
336	F39	O	LVDS_P<47>	Sub-LVDS data positive channel 47	Sub-LVDS output
337	F40	O	LVDS_P<45>	Sub-LVDS data positive channel 45	Sub-LVDS output
338	F41	O	LVDS_P<43>	Sub-LVDS data positive channel 43	Sub-LVDS output
339	F42	O	LVDS_P<41>	Sub-LVDS data positive channel 41	Sub-LVDS output
340	F43	O	LVDS_P<38>	Sub-LVDS data positive channel 38	Sub-LVDS output
341	F44	O	LVDS_P<35>	Sub-LVDS data positive channel 35	Sub-LVDS output
342	F45	-	NC	N/A	Leave floating
343	F46	O	LVDS_P<31>	Sub-LVDS data positive channel 31	Sub-LVDS output
344	F47	O	LVDS_P<29>	Sub-LVDS data positive channel 29	Sub-LVDS output
345	F48	O	LVDS_P<27>	Sub-LVDS data positive channel 27	Sub-LVDS output
346	F49	O	LVDS_P<25>	Sub-LVDS data positive channel 25	Sub-LVDS output
347	F50	O	LVDS_P<22>	Sub-LVDS data positive channel 22	Sub-LVDS output
348	F51	-	NC	N/A	Leave floating
349	F52	O	LVDS_P<18>	Sub-LVDS data positive channel 18	Sub-LVDS output
350	F53	-	NC	N/A	Leave floating
351	F54	O	LVDS_P<14>	Sub-LVDS data positive channel 14	Sub-LVDS output
352	F55	O	LVDS_P<11>	Sub-LVDS data positive channel 11	Sub-LVDS output
353	F56	O	LVDS_P<7>	Sub-LVDS data positive channel 7	Sub-LVDS output
354	F57	O	LVDS_P<5>	Sub-LVDS data positive channel 5	Sub-LVDS output
355	F58	O	LVDS_P<3>	Sub-LVDS data positive channel 3	Sub-LVDS output
356	F59	O	LVDS_P<1>	Sub-LVDS data positive channel 1	Sub-LVDS output
357	F60	O	LVDS_P<0>	Sub-LVDS data positive channel 0	Sub-LVDS output
358	G2	POWER	VAGL	Pixel supply (current sink)	Supply
359	G3	POWER	VAGH	Pixel supply (current source)	Supply
360	G4	GND	GNDA	Ground	Ground
361	G5	POWER	VDDA	Analog supply	Supply
362	G6	POWER	VTXH	Pixel supply (current source)	Supply
363	G7	POWER	VTXL	Pixel supply (current sink)	Supply
364	G8	POWER	VSELH	Pixel supply (current source)	Supply
365	G9	POWER	VABGN	Pixel supply (current source& current sink)	Supply
366	G10	POWER	VAGL	Pixel supply (current sink)	Supply
367	G11	POWER	VAGH	Pixel supply (current source)	Supply
368	G12	POWER	VABG	Pixel supply (current source& current sink)	Supply
369	G13	POWER	VAGL	Pixel supply (current sink)	Supply
370	G14	POWER	VRSTH	Pixel supply (current source& current sink)	Supply
371	G15	POWER	VRSTL	Pixel supply (current source& current sink)	Supply
372	G16	GND	GNDD	Ground	Ground

373	G17	POWER	VDDD	Digital supply	Supply
374	G18	GND	PSUB	Pixel ground	Ground
375	G19	POWER	VAGL	Pixel supply (current sink)	Supply
376	G20	POWER	VAGH	Pixel supply (current source)	Supply
377	G21	POWER	VAGL	Pixel supply (current sink)	Supply
378	G22	POWER	VAGH	Pixel supply (current source)	Supply
379	G23	I/O	VRPC	On-chip generated bias voltage	Bias
380	G24	I/O	VRINIT	On-chip generated bias voltage	Bias
381	G25	I/O	VAGBN	On-chip generated bias voltage	Bias
382	G26	I/O	VAGBP	On-chip generated bias voltage	Bias
383	G27	I/O	VRCN	On-chip generated bias voltage	Bias
384	G28	I/O	VRBP	On-chip generated bias voltage	Bias
385	G29	POWER	VAGL	Pixel supply (current sink)	Supply
386	G30	POWER	VAGH	Pixel supply (current source)	Supply
387	G31	I/O	VCBP1	On-chip generated bias voltage	Bias
388	G32	POWER	VAGL	Pixel supply (current sink)	Supply
389	G33	POWER	VAGH	Pixel supply (current source)	Supply
390	G34	I/O	VCBP2	On-chip generated bias voltage	Bias
391	G35	I/O	VBGBN	On-chip generated bias voltage	Bias
392	G36	I/O	VBGBP	On-chip generated bias voltage	Bias
393	G37	POWER	VAGL	Pixel supply (current sink)	Supply
394	G38	GND	PSUB	Pixel ground	Ground
395	G39	POWER	VAGL	Pixel supply (current sink)	Supply
396	G40	POWER	VAGH	Pixel supply (current source)	Supply
397	G41	POWER	VDDSF	Pixel supply	Supply
398	G42	I/O	VCLBP	On-chip generated bias voltage	Bias
399	G43	I/O	VCLBN	On-chip generated bias voltage	Bias
400	G44	POWER	VBGL	Pixel supply (current sink)	Supply
401	G45	POWER	VBGH	Pixel supply (current source)	Supply
402	G46	POWER	VAGL	Pixel supply (current sink)	Supply
403	G47	POWER	VAGH	Pixel supply (current source)	Supply
404	G48	POWER	VAGL	Pixel supply (current sink)	Supply
405	G49	POWER	VABD	Pixel supply (current source& current sink)	Supply
406	G50	GND	GNDA	Ground	Ground
407	G51	POWER	VDDA	Analog supply	Supply
408	G52	GND	PSUB	Pixel ground	Ground
409	G53	POWER	VAGL	Pixel supply (current sink)	Supply
410	G54	POWER	VAGH	Pixel supply (current source)	Supply
411	G55	POWER	VDDPIX	Pixel supply	Supply
412	G56	GND	GNDD	Ground	Ground
413	G57	POWER	VDDD	Digital supply	Supply
414	G58	O	TDIG2	Digital test signal output	Digital output

415	G59	O	TDIG1	Digital test signal output	Digital output

Electrical Characteristics

DC Characteristics

Table 2 DC characteristics

Item		Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog	VDDA		3.25	3.3	3.35	V
		VDDPLL		1.45	1.5	1.55	V
	Digital	VDDAD		1.63	1.65	1.67	V
		VDDD		1.55	1.6	1.65	V
	IO ring	VDDIO		3.2	3.3	3.4	V
	Pixel	VDDSF		3.25	3.3	3.35	V
		VDDPIX		3.25	3.3	3.35	V
		VAGH		2.95	3.0	3.05	V
		VAGL		-0.55	-0.5	-0.45	V
		VBGH		2.95	3.0	3.05	V
		VBGL		-0.55	-0.5	-0.45	V
		VTXH		2.95	3.0	3.05	V
		VTXL		-0.05	0	0	V
		VABG		2.95	3.0	3.05	V
		VABGN		3.25	3.3	3.35	V
		VABD		3.25	3.3	3.35	V
		VRSTH		3.55	3.6	3.63	V
		VRSTL		0.45	0.5	0.55	V
		VSELH		3.25	3.3	3.35	V
		VDDPS		3.25	3.3	3.35	V
Digital Input		SPI_CS_N SPI_IN SPI_CLK TRIG SYS_RST_N CLK_REF	V_{IH}	0.8 x VDDIO	VDDIO	VDDIO + 0.3	V
			V_{IL}	0	0	0.3	V
Digital Output		SPI_OUT TDIG1 TDIG2	V_{OH}		VDDIO		V
			V_{OL}	0	0	0.3	V
Sub-LVDS Output		DDR_P<0:3> DDR_N <0:3> LVDS_P<0:145> LVDS_N<0:145>	V_{CM}		0.9		V
			V_{OD}	0.1	0.15	0.2	V

NOTE:

1) DDR_P/N<0> is the DDR clock for LVDS_P/N<0:35>; DDR_P/N<1> is the DDR clock for LVDS_P/N<37:71>; DDR_P/N<2> is the DDR clock for LVDS_P/N<73:107>, DDR_P/N<3> is the DDR clock for LVDS_P/N<109:145>,which can be referred to the section 'Clock Channels'.

AC Characteristics

1. Digital input control signal waveform diagram

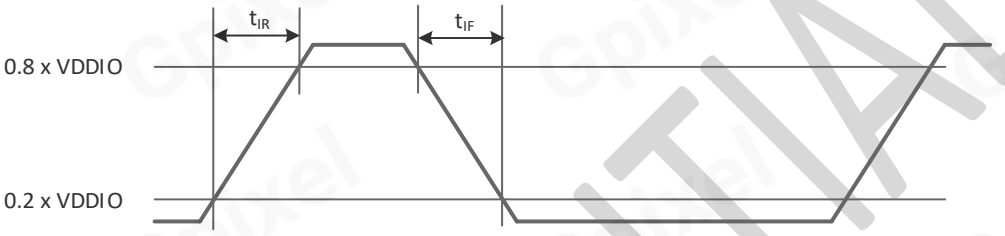


Figure 7 AC digital input control signal

Table 3 AC characteristics for digital input control signals

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Control signal rising edge	t_{IR}	—	3.1	—	ns	Define with 0.2 x VDDIO and 0.8 x VDDIO
Control signal falling edge	t_{IF}	—	2.6	—	ns	Define with 0.2 x VDDIO and 0.8 x VDDIO

2. Digital output signal waveform diagram

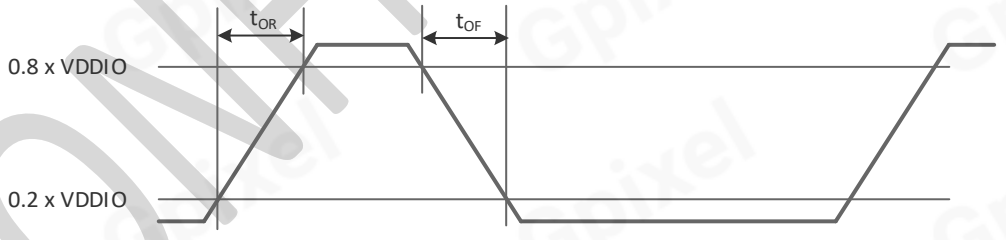


Figure 8 AC digital output signal

Table 4 AC characteristics for digital output signal

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Digital output signal rising edge	t_{OR}	—	5.0	—	ns	Define with 0.2 x VDDIO and 0.8 x VDDIO
Digital output signal falling edge	t_{OF}	—	1.1	—	ns	Define with 0.2 x VDDIO and 0.8 x VDDIO

NOTE:

1) Output load capacitance < 18pF.

3. Sub-LVDS driver output signal waveform diagram

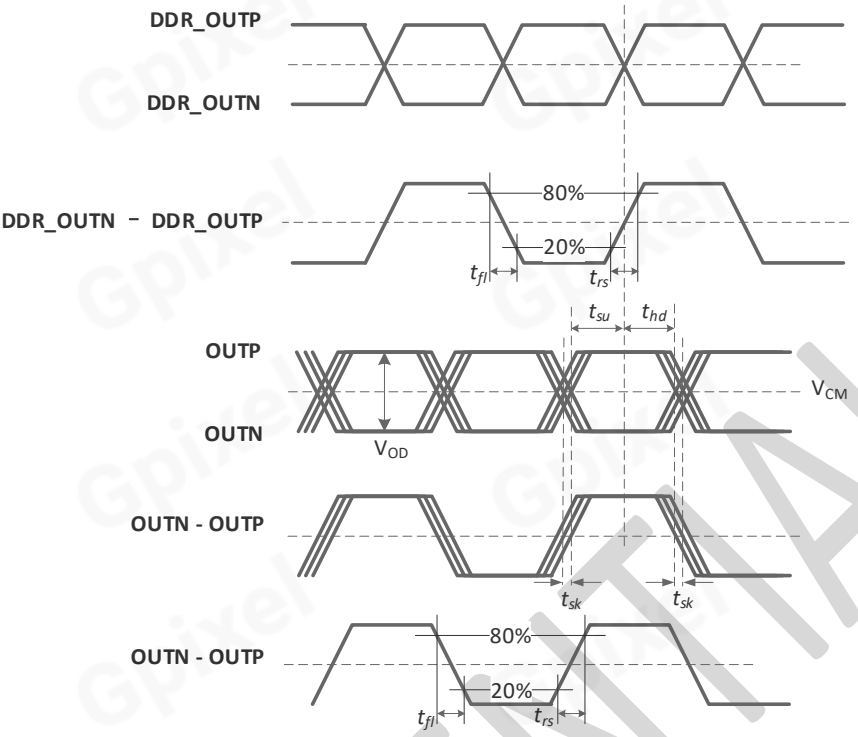


Figure 9 Sub-LVDS driver output

Table 5 Sub-LVDS driver output

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock Duty Cycle		40	50	60	%	DDR clock 480MHz
Data setup time	t_{su}	T.B.D	—	—	ps	Data rate 960Mbps
Date hold time	t_{hd}	T.B.D	—	—	ps	Data rate 960Mbps
Data skew time	t_{sk}	—	—	T.B.D	ps	Data rate 960Mbps
Data rising time	t_{rs}	—	T.B.D	—	ps	Simulated value with load capacitance (TBD pF)
Data falling time	t_{fl}	—	T.B.D	—	ps	Simulated value with load capacitance (TBD pF)
Differential output voltage	V_{OD}	100	150	200	mV	
Output common mode voltage	V_{CM}	0.8	0.9	1.0	V	

NOTE:

1) Output load capacitance < 8pF.

Power Consumption

Table 6 Power consumption for P1 10-bit and P1 12-bit mode

Supply source	Typical voltage(V)	10-bit mode			12-bit mode		
		Average current (mA)	Peak current (mA)	Average power consumption (mW)	Average current (mA)	Peak current (mA)	Average power consumption(mW)
VDDA	3.3	703	711	2319.9	571	572	1884.3
VDDPLL	1.5	<5	<5		<10	<10	
VDDAD	1.65	548	586	904.2	924	1026	1524.6
VDDD	1.6	1228	1240	1964.8	1425	1433	2280.0
VDDIO	3.3	<5	<5		<5	<5	
VDDSF	3.3	213	246	702.9	153	156	504.9
VDDPIX	3.3	<5	<5		<5	<5	
VAGH	3.0	95	380	285.0	88	266	264.0
VAGL	-0.5	-96	-365	48.0	-96	-252	48.0
VBGH	3.0	<5	<5		<5	<10	
VBGL	-0.5	>-5	>-10		>-5	>-10	
VTXH	3.0	<5	<5		<5	<5	
VTXL	0	>-5	>-5		>-5	>-5	
VABG	3.0	<5	<5		<5	<5	
VABGN	3.3	<5	<5		<5	<5	
VABD	3.3	<5	<5		<5	<5	
VRSTH	3.6	<5	<5		<5	<5	
VRSTL	0.5	>-5	>-5		>-5	>-5	
VSELH	3.3	<5	<5		<5	<5	
VDDPS	3.3	<5	<5		<5	<5	
Total power consumption (mW)				6224.8			6505.8

NOTE:

1) The negative sign in the current value represents the current sink.

Image Sensor Characteristics

Key Specification

Table 7 Key performance for GLT5016BSI P1 12bit 500kHz

Item	Min.	Typ.	Max.	Unit	Note
Conversion factor		0.23		DN/e^-	
Full well capacity	TBD	15.2		ke^-	1
Non-linearity error		0.2	TBD	%	2
Max. SNR		41.8		dB	
Temporal dark noise		7.5	TBD	e^-	3
Dynamic range		66.1		dB	4
DSNU		2.1	TBD	e^-	6
PRNU		0.3	TBD	%	6
Vertical Charge Transfer Efficiency	> 0.99999				7

Table 8 Key performance for GLT5016BSI P1 10bit 500kHz

Item	Min.	Typ.	Max.	Unit	Note
Conversion factor		0.045		DN/e^-	
Full well capacity	TBD	16.3		ke^-	1
Non-linearity error		0.2	TBD	%	2
Max. SNR		42.1		dB	
Temporal dark noise		15.3	TBD	e^-	3
Dynamic range		60.5		dB	4
Peak QE @ 460nm		94.2		%	10
Sensitivity @ 460nm		$5.5x10^7$		$e^-/((W/m^2)\cdot s)$	10
Dark current		0.97		$ke^-/s/pix$	5
DSNU		9.3	TBD	e^-	6
PRNU		0.3	TBD	%	6
Vertical Charge Transfer Efficiency	> 0.99999				7

NOTE:

1. Full well capacity (FWC) is calculated by dividing the saturation level (DN) by the conversion factor (DN/e-).
2. Non-linearity error is calculated in the range between 5-95% of the saturation level.
3. Temporal dark noise is the mean value of the whole pixel array.
4. The dynamic range is the ratio of FWC (e-) to temporal dark noise (e-) measured at the same system gain setting, the unit of dB is 20 x log (DR).
5. Dark current is measured at environment temperature of -15°C, and the die temperature for this measurement is around 15°C obtained by calibration of the die temperature sensor.
6. DSNU and PRNU results are both measured with full scale image without defect columns, which are both with

high-pass filtering.

7. The pixel signal value is controlled near 50% full well signal for Vertical Charge Transfer Efficiency test.
8. All test results are measured at room temperature of 25°C, the die temperature is around 65°C.
9. All measurement methods are based on the EMVA Standard 1288 (Release 4.0) if no special noted.
10. Peak QE and sensitivity are tested on the visible and NIR range optimized version of the chip.

Temporal Dark Noise Distribution

The curves below show the cumulative histogram for temporal dark noise distribution at P1 10-bit mode and P1 12-bit mode.

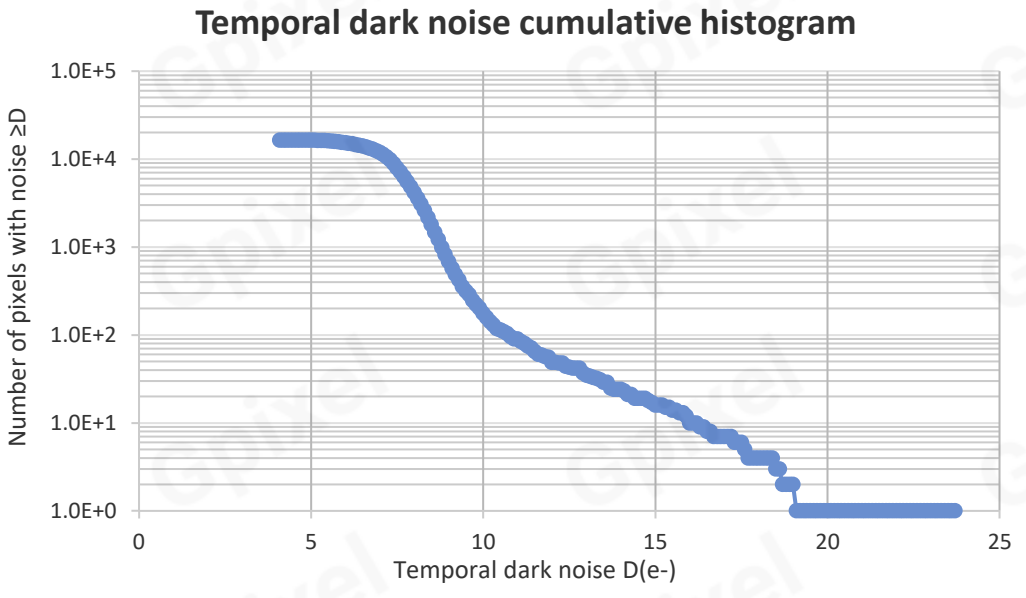


Figure 10 Temporal dark noise distribution for P1 12-bit mode

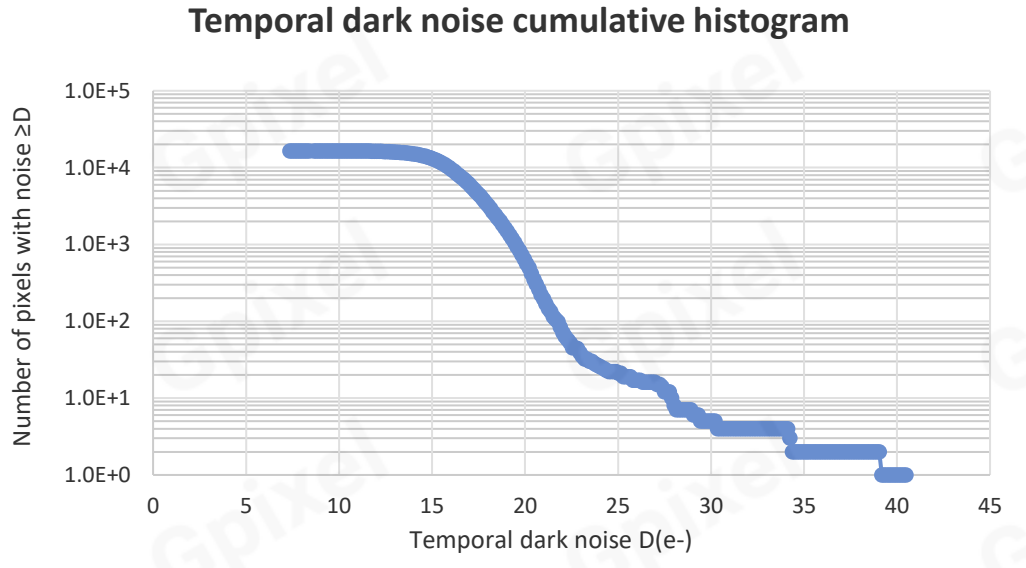


Figure 11 Temporal dark noise distribution for P1 10-bit mode

Spectral Sensitivity Characteristics

GLT5016BSI comes in 2 spectrum variants: an UV-optimized with high QE below 300 nm (GLT5016BSI-AUM) and a visible and NIR range optimized version (GLT5016BSI-ABM).

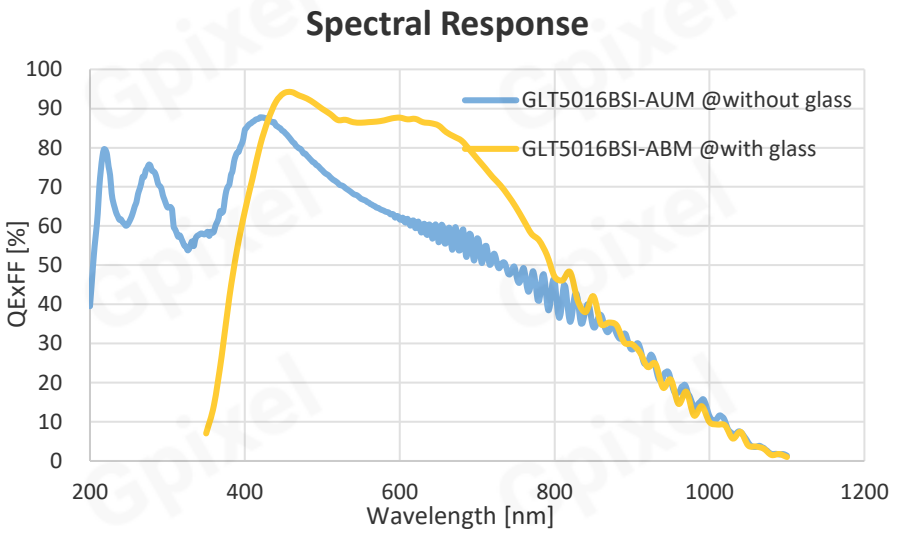


Figure 12 Spectral Sensitivity Characteristics

The table below shows more details about the QE measurement results.

Table 9 Detailed QE measurement results

Wavelength (nm)	GLT5016BSI-AUM QE x FF (%)	Wavelength (nm)	GLT5016BSI-ABM QE x FF (%)
200	39.52	-	-
266	70.76	-	-
250	60.85	-	-
300	64.79	-	-
350	58.16	350	7.04
400	84.57	400	63.82
420	87.79	450	93.87
450	84.19	460	94.22
500	74.22	500	89.90
550	66.97	550	86.38
600	61.67	600	87.68
650	55.92	650	85.67
700	56.82	700	77.17
750	47.97	750	64.82
800	46.12	800	47.07
850	34.21	850	42.08
900	28.48	900	29.80
950	20.65	950	20.80
1000	11.42	1000	9.92
1050	4.70	1050	3.94
1100	1.35	1100	1.00

NOTE:

1) GLT5016BSI-AUM QE is measured without the glass cover on sensor.
2) GLT5016BSI-ABM QE is measured with the glass cover on sensor.

Dark Current with Different Die Temperature

Dark current test results with different temperature for P1 10-bit mode are shown below. The die temperature is measured with an on-chip temperature sensor. See chapter of 'Temperature Readout' for details.

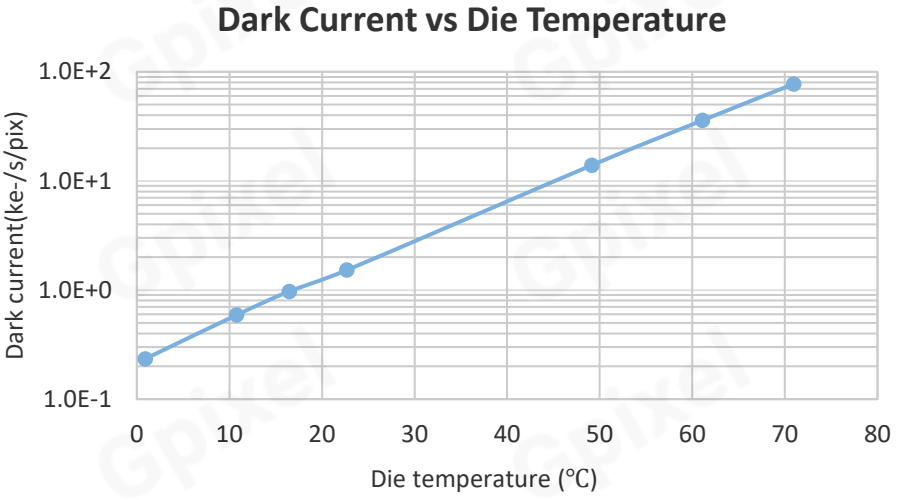


Figure 13 Dark current with different die temperature

The graph below shows the dark current distribution of the sensor tested at 15°C of die temperature for P1 10-bit mode. The dark current value with the most pixel counts is around 0.97ke-/s/pix.

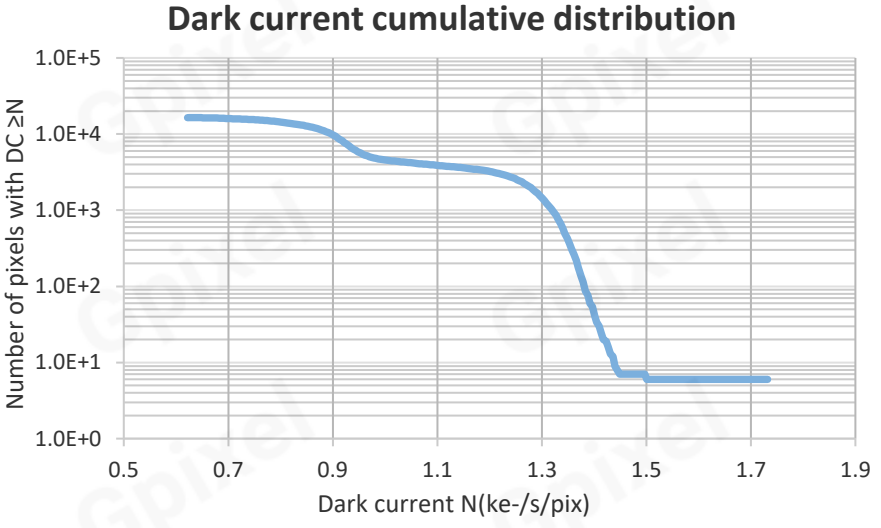


Figure 14 Dark current cumulative distribution

Register Map

Table 10 gives the register setting of GLT5016BSI for P1 12bit 500kHz.

Table 11 gives the register setting of GLT5016BSI for P1 10bit 500kHz.

Some of the registers may need to be tuned based on specific applications, i.e. the registers described in section 'Sensor Configuration' and 'Description of Various Functions'. These registers have digital setting bits separated in two or more neighbor bytes(Address). In this case, the grouping is always from high to low. For example, register Training pattern is 12-bit shown in Table 10. Its digital bit from high to low is H<106>-Bit <3:0> to H<105>-Bit <7:0>.

Table 10 Register map of GLT5016BSI for P1 12bit 500kHz

Hex address	Hex value	Hex address	Hex value	Hex address	Hex value	Hex address	Hex value
0000	00	0053	4B	00A6	07	00F9	E5
0001	01	0054	9D	00A7	01	00FA	10
0002	00	0055	FF	00A8	06	00FB	32
0003	00	0056	FF	00A9	02	00FC	0A
0004	00	0057	22	00AA	07	00FD	18
0005	00	0058	74	00AB	0A	00FE	AA
0006	01	0059	FF	00AC	1C	00FF	C0
0007	08	005A	FF	00AD	FF	0100	A0
0008	08	005B	3F	00AE	FF	0101	08
0009	05	005C	82	00AF	3C	0102	00
000A	9E	005D	FF	00B0	8C	0103	02
000B	00	005E	FF	00B1	FF	0104	00
000C	FF	005F	53	00B2	FF	0105	65
000D	FF	0060	9B	00B3	FF	0106	01
000E	33	0061	FF	00B4	FF	0107	00
000F	00	0062	FF	00B5	FF	0108	01
0010	02	0063	19	00B6	FF	0109	00
0011	01	0064	66	00B7	02	010A	00
0012	01	0065	FF	00B8	0B	010B	6C
0013	01	0066	FF	00B9	03	010C	00
0014	4A	0067	28	00BA	0C	010D	00
0015	00	0068	78	00BB	07	010E	00
0016	33	0069	FF	00BC	2A	010F	00
0017	06	006A	FF	00BD	FF	0110	00
0018	00	006B	0A	00BE	FF	0111	B3
0019	00	006C	2B	00BF	37	0112	01
001A	0A	006D	FF	00C0	9D	0113	90
001B	62	006E	FF	00C1	FF	0114	01

001C	02	006F	14	00C2	FF	0115	00
001D	01	0070	2E	00C3	07	0116	01
001E	0A	0071	FF	00C4	0C	0117	00
001F	FF	0072	FF	00C5	FF	0118	01
0020	FF	0073	1F	00C6	FF	0119	01
0021	2A	0074	30	00C7	9D	011A	0F
0022	38	0075	FF	00C8	2D	011B	00
0023	FF	0076	FF	00C9	35	011C	01
0024	FF	0077	24	00CA	13	011D	00
0025	FF	0078	33	00CB	9D	011E	00
0026	FF	0079	FF	00CC	0C	011F	01
0027	FF	007A	FF	00CD	FF	0800	B0
0028	FF	007B	FF	00CE	FF	0801	9B
0029	FF	007C	FF	00CF	0C	0802	C3
002A	FF	007D	FF	00D0	13	0803	E5
002B	FF	007E	FF	00D1	2C	0804	8B
002C	FF	007F	FF	00D2	33	0805	F0
002D	FF	0080	FF	00D3	01	0806	C3
002E	FF	0081	FF	00D4	06	0807	9C
002F	FF	0082	FF	00D5	2D	0808	53
0030	FF	0083	FF	00D6	31	0809	53
0031	3C	0084	FF	00D7	2E	080A	A1
0032	8D	0085	FF	00D8	30	080B	50
0033	FF	0086	FF	00D9	9B	080C	5D
0034	FF	0087	FF	00DA	9C	080D	CF
0035	FF	0088	FF	00DB	9C	080E	DE
0036	FF	0089	FF	00DC	9D	080F	E3
0037	FF	008A	FF	00DD	FF	0810	DA
0038	FF	008B	FF	00DE	FF	0811	53
0039	FF	008C	FF	00DF	FF	0812	58
003A	FF	008D	FF	00E0	FF	0813	ED
003B	4B	008E	FF	00E1	FF	0814	90
003C	9D	008F	FF	00E2	FF	0815	F0
003D	FF	0090	FF	00E3	03	0816	B0
003E	FF	0091	FF	00E4	04	0817	57
003F	22	0092	FF	00E5	FF	0818	21
0040	74	0093	FF	00E6	FF	0819	E6
0041	FF	0094	FF	00E7	15	081A	55
0042	FF	0095	FF	00E8	2A	081B	D5
0043	4B	0096	FF	00E9	FF	081C	6E

0044	9D	0097	FF	00EA	FF	081D	2C
0045	FF	0098	FF	00EB	30	081E	56
0046	FF	0099	FF	00EC	9D	081F	03
0047	22	009A	FF	00ED	FF	0820	00
0048	74	009B	FF	00EE	FF	0821	00
0049	FF	009C	FF	00EF	FF	1401	00
004A	FF	009D	FF	00F0	FF	1402	00
004B	4B	009E	FF	00F1	FF	1403	01
004C	9D	009F	FF	00F2	FF	1404	34
004D	FF	00A0	FF	00F3	7F	1405	08
004E	FF	00A1	FF	00F4	1E	1406	06
004F	22	00A2	FF	00F5	24	1407	00
0050	74	00A3	01	00F6	F8		
0051	FF	00A4	06	00F7	41		
0052	FF	00A5	02	00F8	5A		

Table 11 Register map of GLT5016BSI for P1 10bit 500kHz

Hex address	Hex value	Hex address	Hex value	Hex address	Hex value	Hex address	Hex value
0000	00	0053	2C	00A6	06	00F9	E4
0001	01	0054	5C	00A7	01	00FA	09
0002	00	0055	FF	00A8	05	00FB	32
0003	00	0056	FF	00A9	02	00FC	0A
0004	00	0057	16	00AA	06	00FD	18
0005	00	0058	41	00AB	06	00FE	7C
0006	01	0059	FF	00AC	0F	00FF	C1
0007	08	005A	FF	00AD	FF	0100	A0
0008	08	005B	21	00AE	FF	0101	08
0009	05	005C	4D	00AF	20	0102	00
000A	5E	005D	FF	00B0	57	0103	00
000B	00	005E	FF	00B1	FF	0104	00
000C	FF	005F	2C	00B2	FF	0105	65
000D	FF	0060	5A	00B3	FF	0106	01
000E	29	0061	FF	00B4	FF	0107	00
000F	00	0062	FF	00B5	FF	0108	01
0010	02	0063	10	00B6	FF	0109	00
0011	01	0064	48	00B7	01	010A	00
0012	01	0065	FF	00B8	06	010B	00
0013	01	0066	FF	00B9	02	010C	00
0014	4A	0067	18	00BA	07	010D	00

0015	00	0068	50	00BB	03	010E	00
0016	33	0069	FF	00BC	19	010F	01
0017	06	006A	FF	00BD	FF	0110	00
0018	00	006B	06	00BE	FF	0111	78
0019	00	006C	1C	00BF	1F	0112	00
001A	0A	006D	FF	00C0	5B	0113	20
001B	62	006E	FF	00C1	FF	0114	00
001C	02	006F	0C	00C2	FF	0115	00
001D	01	0070	1E	00C3	01	0116	01
001E	06	0071	FF	00C4	05	0117	00
001F	FF	0072	FF	00C5	FF	0118	03
0020	FF	0073	12	00C6	FF	0119	01
0021	1B	0074	20	00C7	0B	011A	0F
0022	2B	0075	FF	00C8	1A	011B	01
0023	FF	0076	FF	00C9	21	011C	01
0024	FF	0077	18	00CA	5C	011D	00
0025	FF	0078	22	00CB	05	011E	00
0026	FF	0079	FF	00CC	58	011F	00
0027	FF	007A	FF	00CD	FF	0800	B0
0028	FF	007B	FF	00CE	FF	0801	9B
0029	FF	007C	FF	00CF	05	0802	C3
002A	FF	007D	FF	00D0	09	0803	E4
002B	FF	007E	FF	00D1	19	0804	83
002C	FF	007F	FF	00D2	20	0805	F0
002D	FF	0080	FF	00D3	01	0806	C3
002E	FF	0081	FF	00D4	02	0807	9C
002F	FF	0082	FF	00D5	1C	0808	53
0030	FF	0083	FF	00D6	1D	0809	53
0031	20	0084	FF	00D7	1A	080A	BB
0032	59	0085	FF	00D8	1C	080B	50
0033	FF	0086	FF	00D9	5B	080C	5D
0034	FF	0087	FF	00DA	5D	080D	CF
0035	FF	0088	FF	00DB	5C	080E	EE
0036	FF	0089	FF	00DC	5D	080F	F7
0037	FF	008A	FF	00DD	FF	0810	DA
0038	FF	008B	FF	00DE	FF	0811	53
0039	FF	008C	FF	00DF	FF	0812	58
003A	FF	008D	FF	00E0	FF	0813	DD
003B	2C	008E	FF	00E1	FF	0814	A0
003C	5C	008F	FF	00E2	FF	0815	F0

003D	FF	0090	FF	00E3	03	0816	B0
003E	FF	0091	FF	00E4	04	0817	57
003F	16	0092	FF	00E5	FF	0818	21
0040	41	0093	FF	00E6	FF	0819	D9
0041	FF	0094	FF	00E7	0B	081A	5B
0042	FF	0095	FF	00E8	1A	081B	D5
0043	2C	0096	FF	00E9	FF	081C	6E
0044	5C	0097	FF	00EA	FF	081D	2C
0045	FF	0098	FF	00EB	1F	081E	72
0046	FF	0099	FF	00EC	5D	081F	03
0047	16	009A	FF	00ED	FF	0820	00
0048	41	009B	FF	00EE	FF	0821	00
0049	FF	009C	FF	00EF	FF	1401	00
004A	FF	009D	FF	00F0	FF	1402	00
004B	2C	009E	FF	00F1	FF	1403	01
004C	5C	009F	FF	00F2	FF	1404	34
004D	FF	00A0	FF	00F3	FF	1405	08
004E	FF	00A1	FF	00F4	1F	1406	06
004F	16	00A2	FF	00F5	24	1407	00
0050	41	00A3	01	00F6	F8		
0051	FF	00A4	05	00F7	21		
0052	FF	00A5	02	00F8	B0		

Driving the Sensor

Sensor Setting Flow

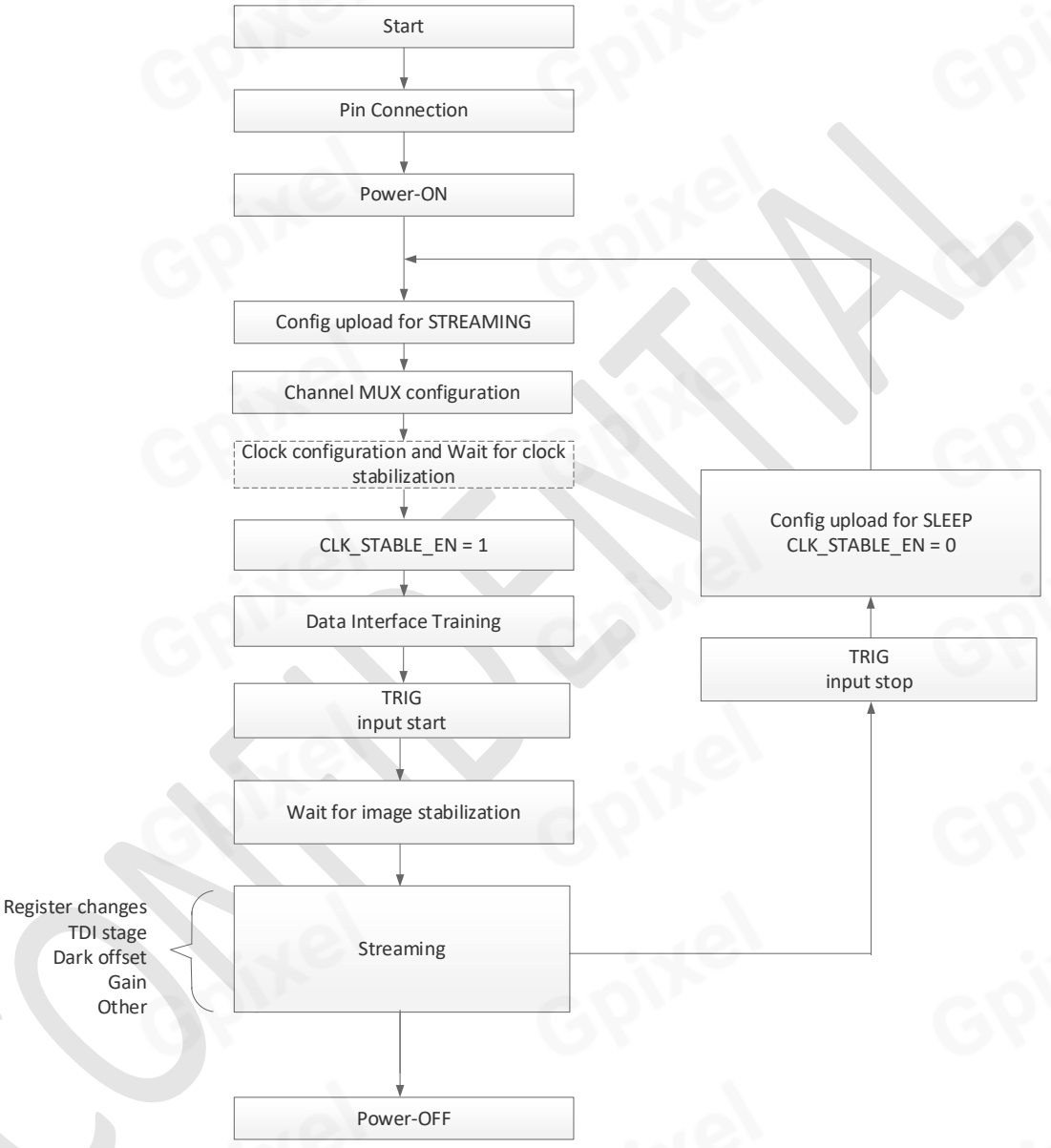


Figure 15 GLT5016BSI setting flow

Registers for 'CLK_STABLE_EN' are described as below:

Table 12 Register description for 'CLK_STABLE_EN'

Address(Hex)	Bit	Name	Description
0	0	CLK_STABLE_EN	0: Disable image capture 1: Enable image capture

Periphery Connections

This section shows the typical examples for hardware connections of GLT5016BSI. They are provided for user's reference, Gpixel does not take any responsibility for use of these circuits.

Analog Power Connections

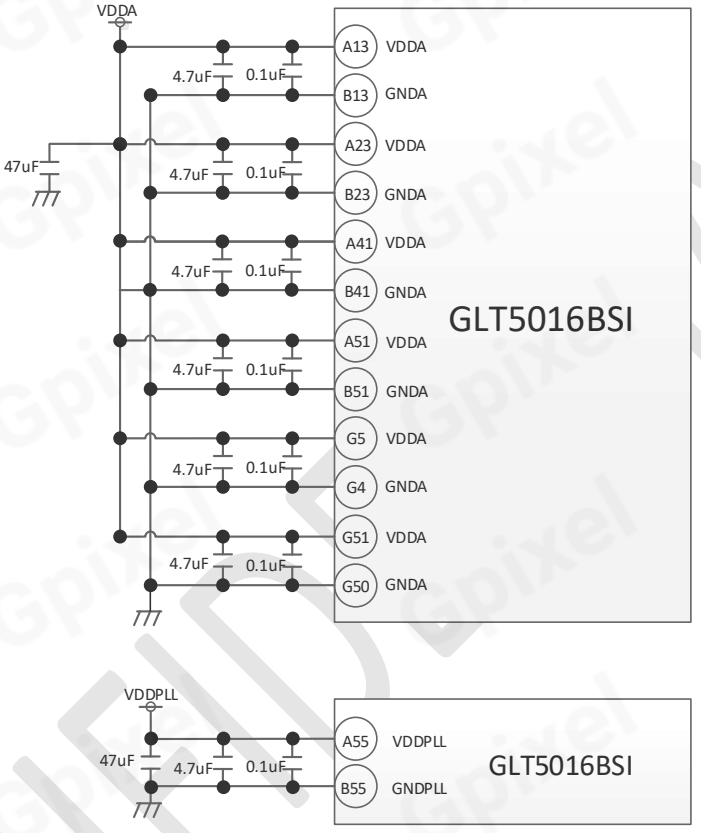


Figure 16 GLT5016BSI analog power connections

NOTE:

1) Avoid using switching power for analog supplies.

Digital Power Connections

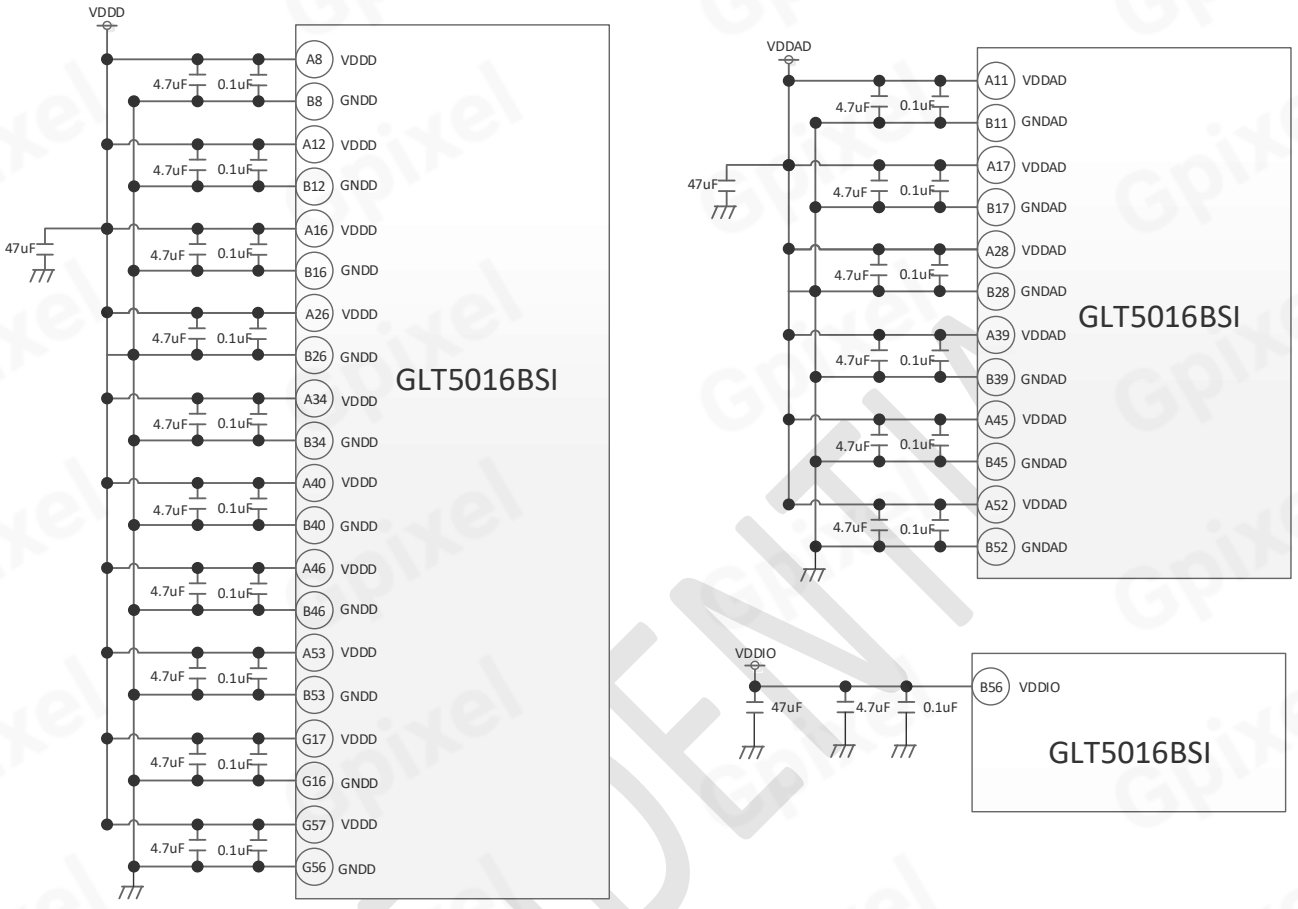


Figure 17 GLT5016BSI digital power connections

NOTE:

1) Avoid using switching power for digital supplies.

Array Supply Connections

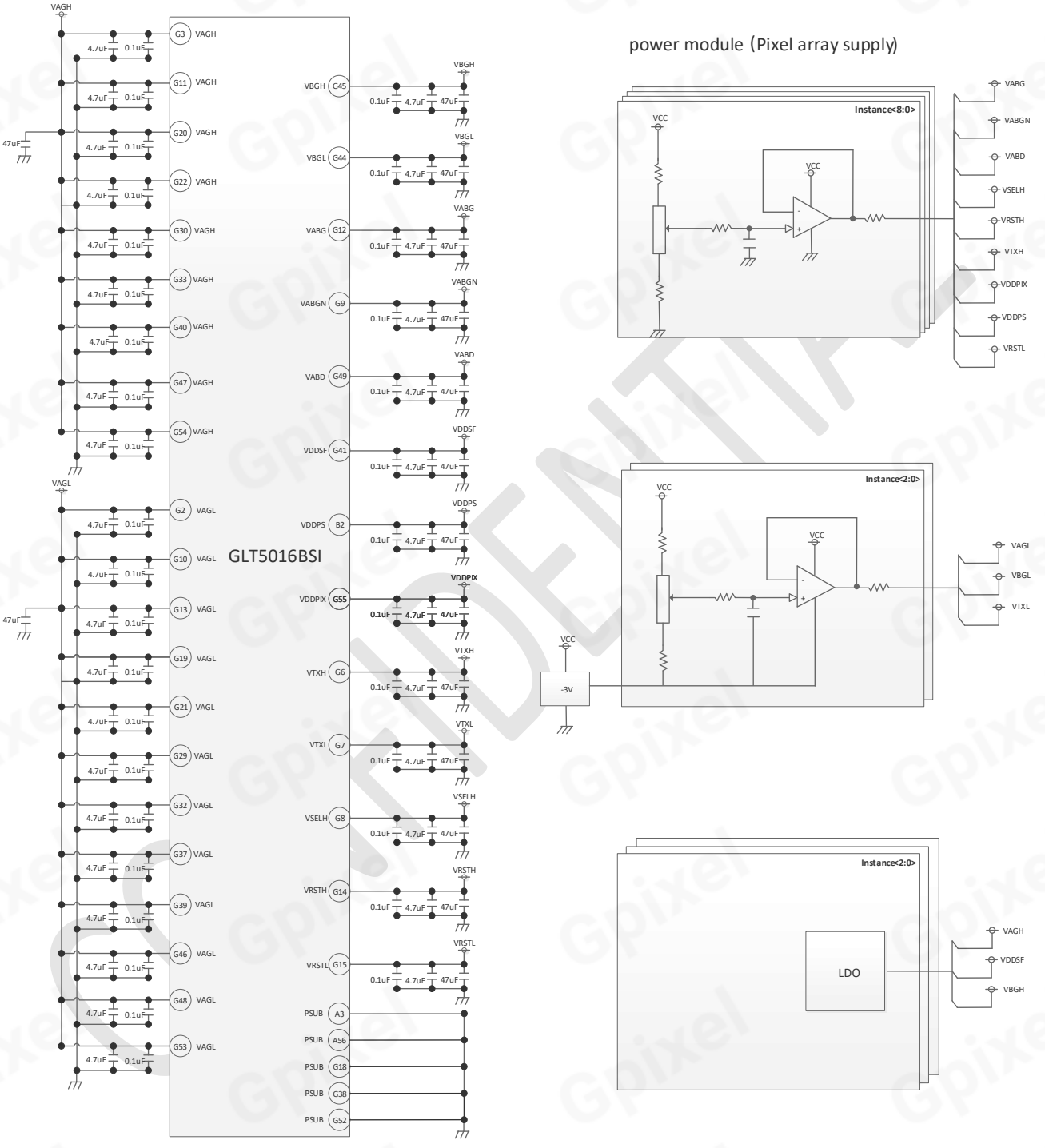


Figure 18 GLT5016BSI pixel array supply connections

Bias Pin Connections

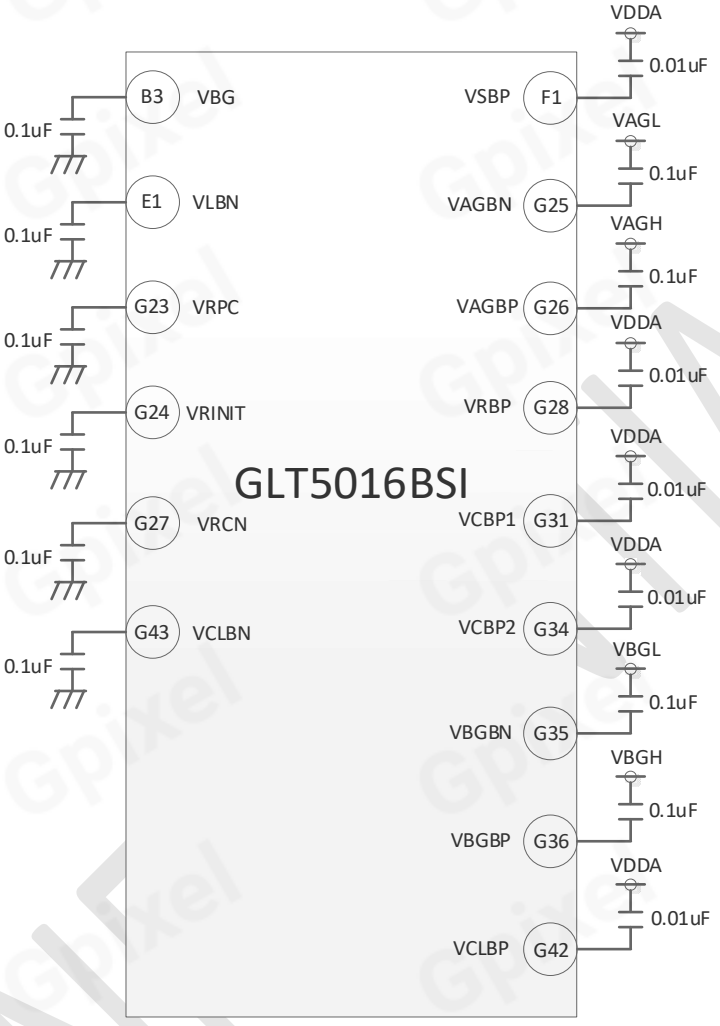


Figure 19 GLT5016BSI bias connections

Analog Temperature Diode Connections

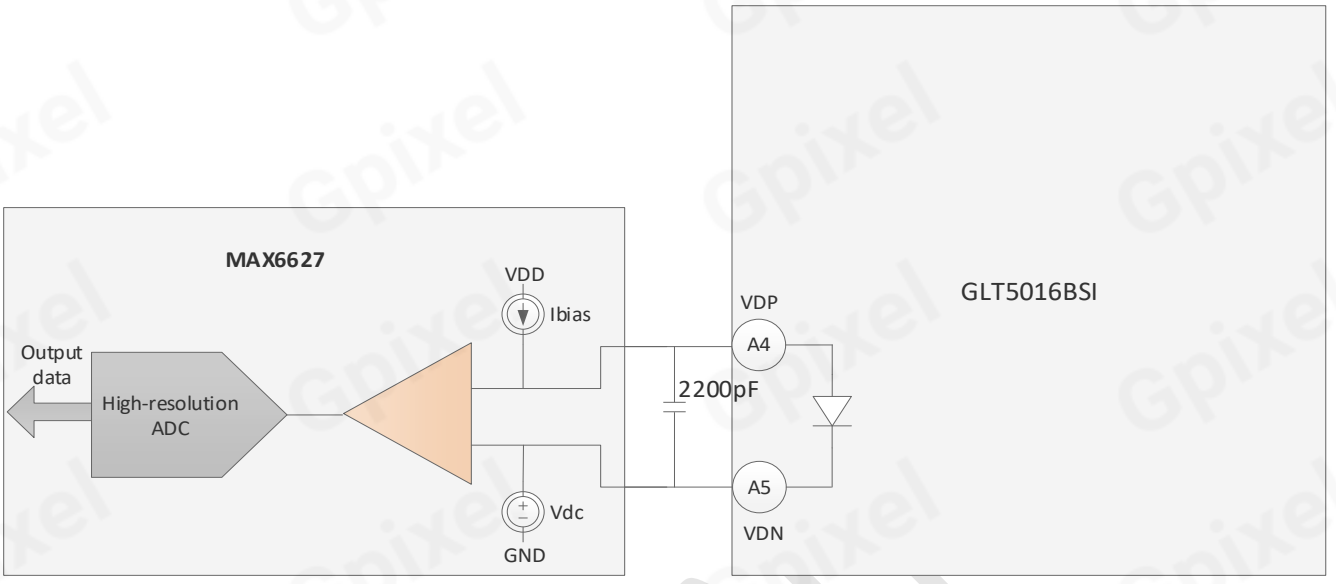


Figure 20 GLT5016BSI analog temperature sensor connections

NOTE:

1) Pin A4 and A5 should be short to GNDA if the temperature sensor is not used.
2) The analog temperature sensor may not be very accurate at high temperatures when used with the MAX6627. It is recommended to prioritize the use of digital temperature sensor. Gpixel is currently verifying the new external connection devise internally and will update datasheet after the verification is completed.

Digital I/O and Clock inputs

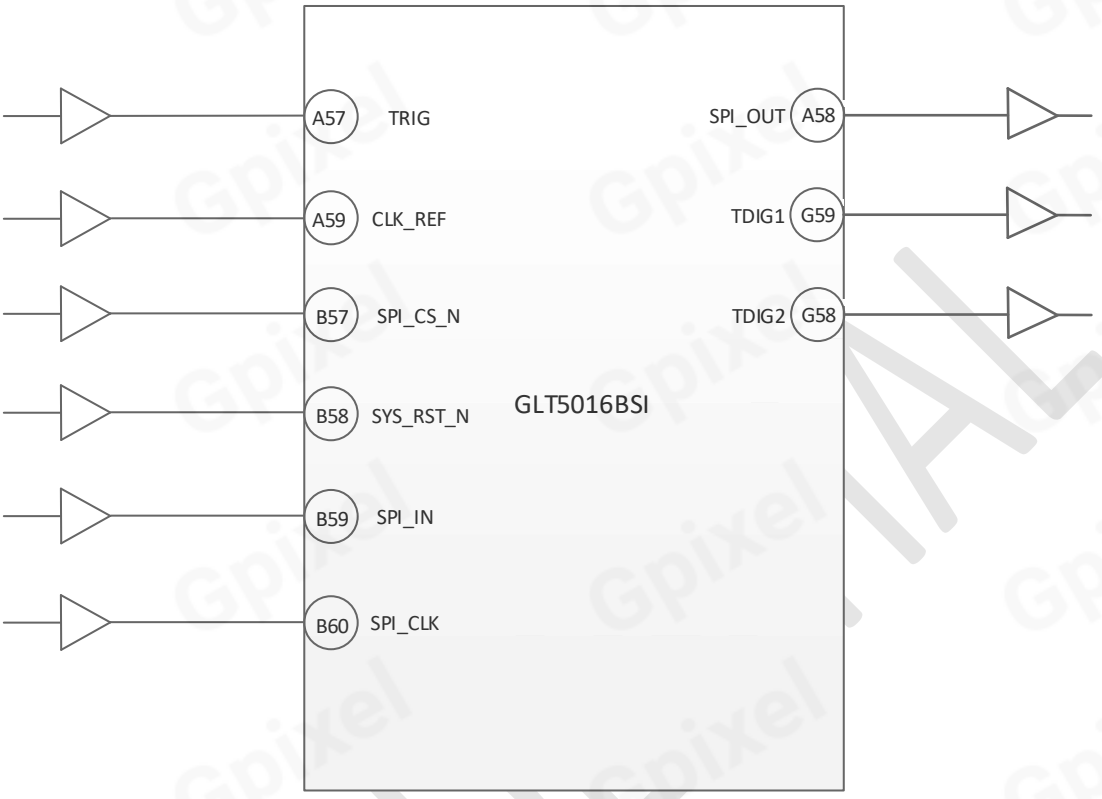
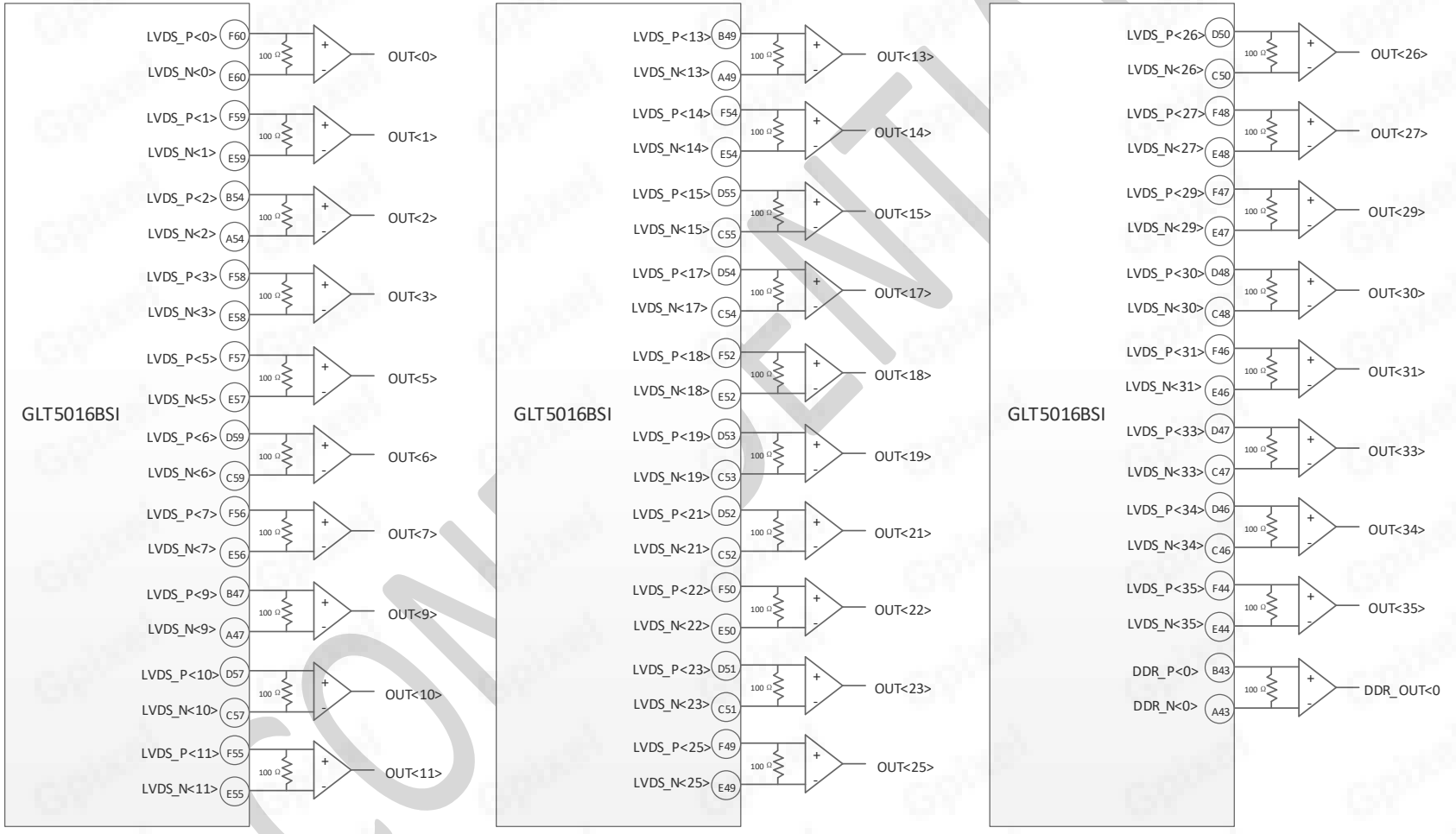
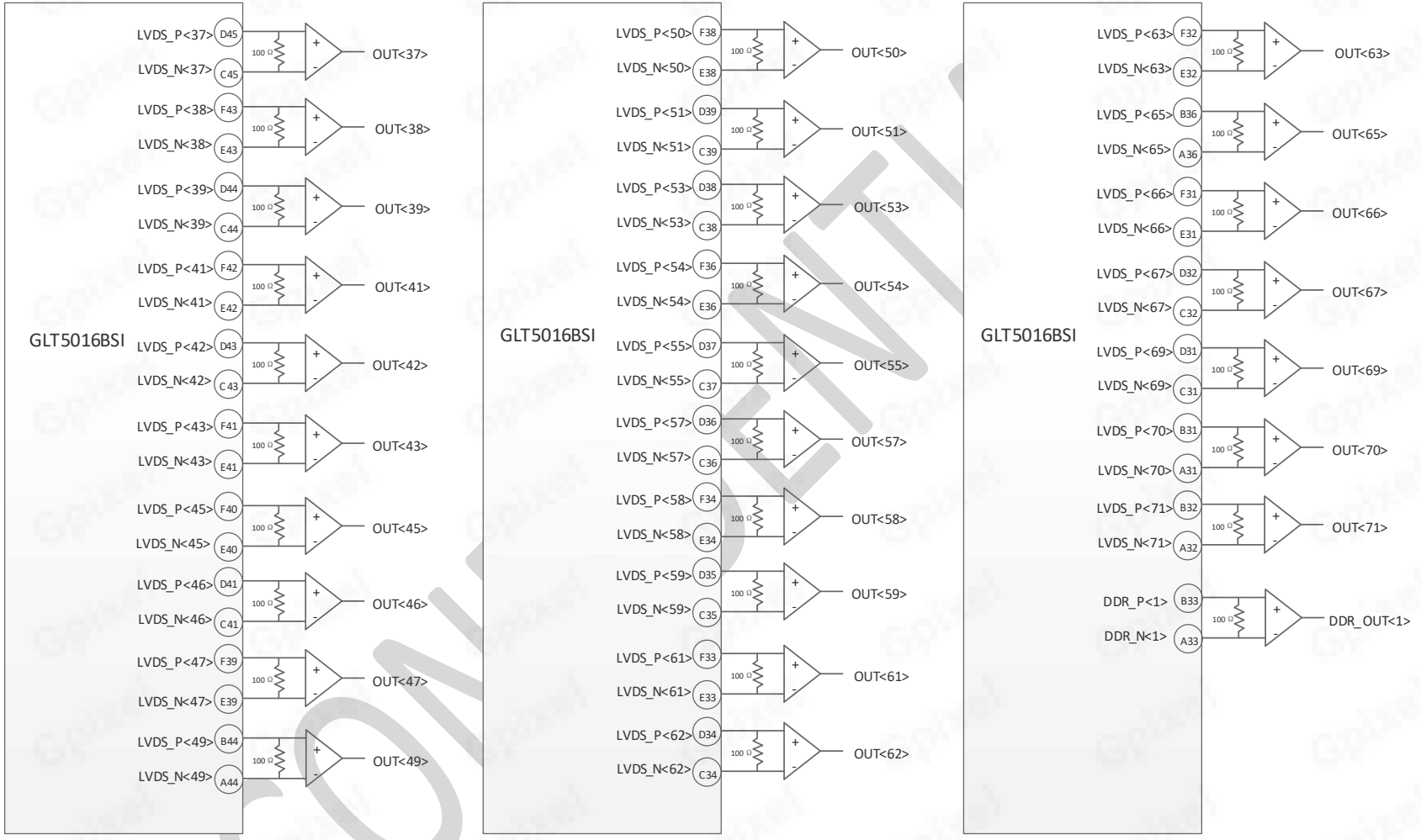
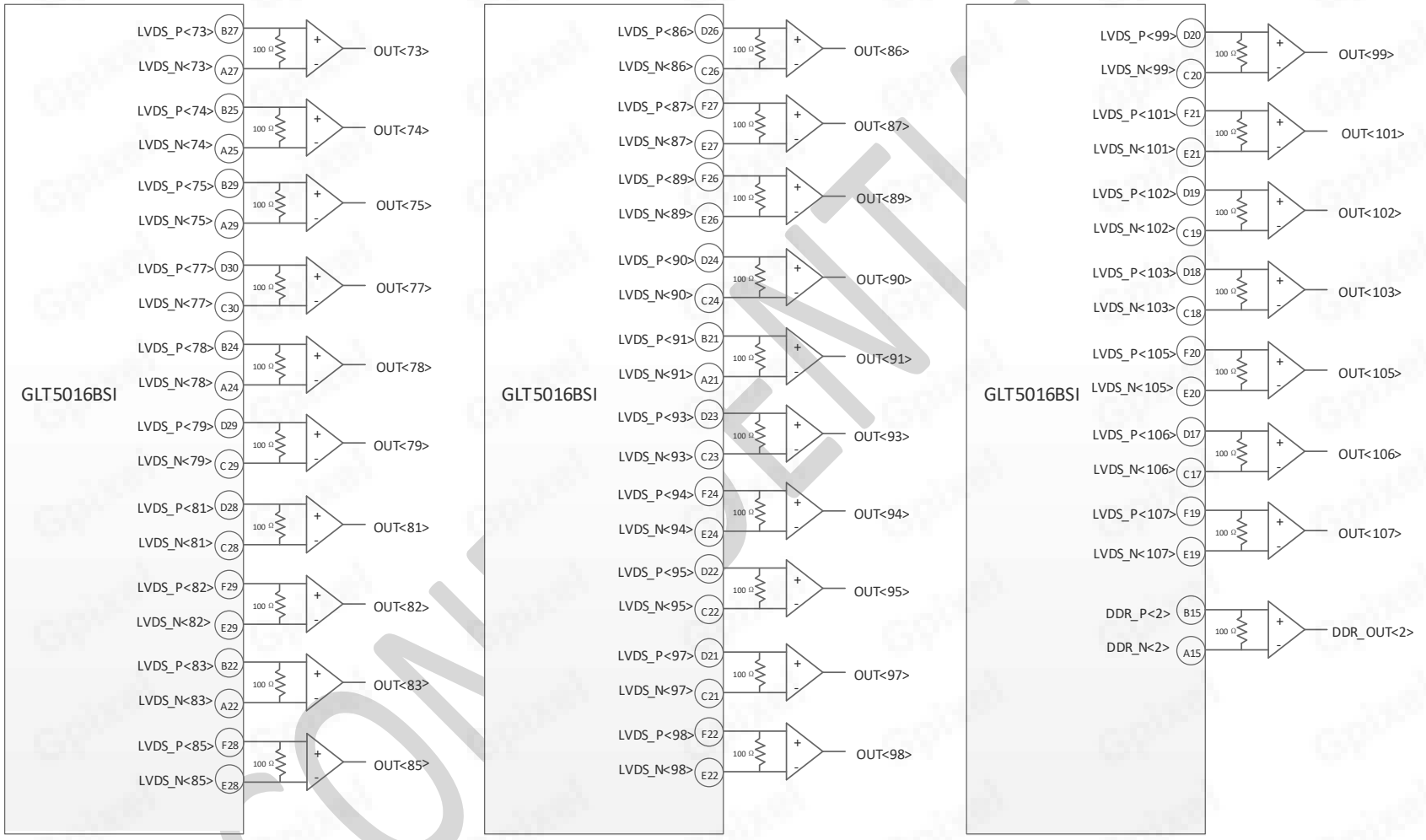


Figure 21 GLT5016BSI digital IO and clock input connections

Sub-LVDS Inputs/Outputs







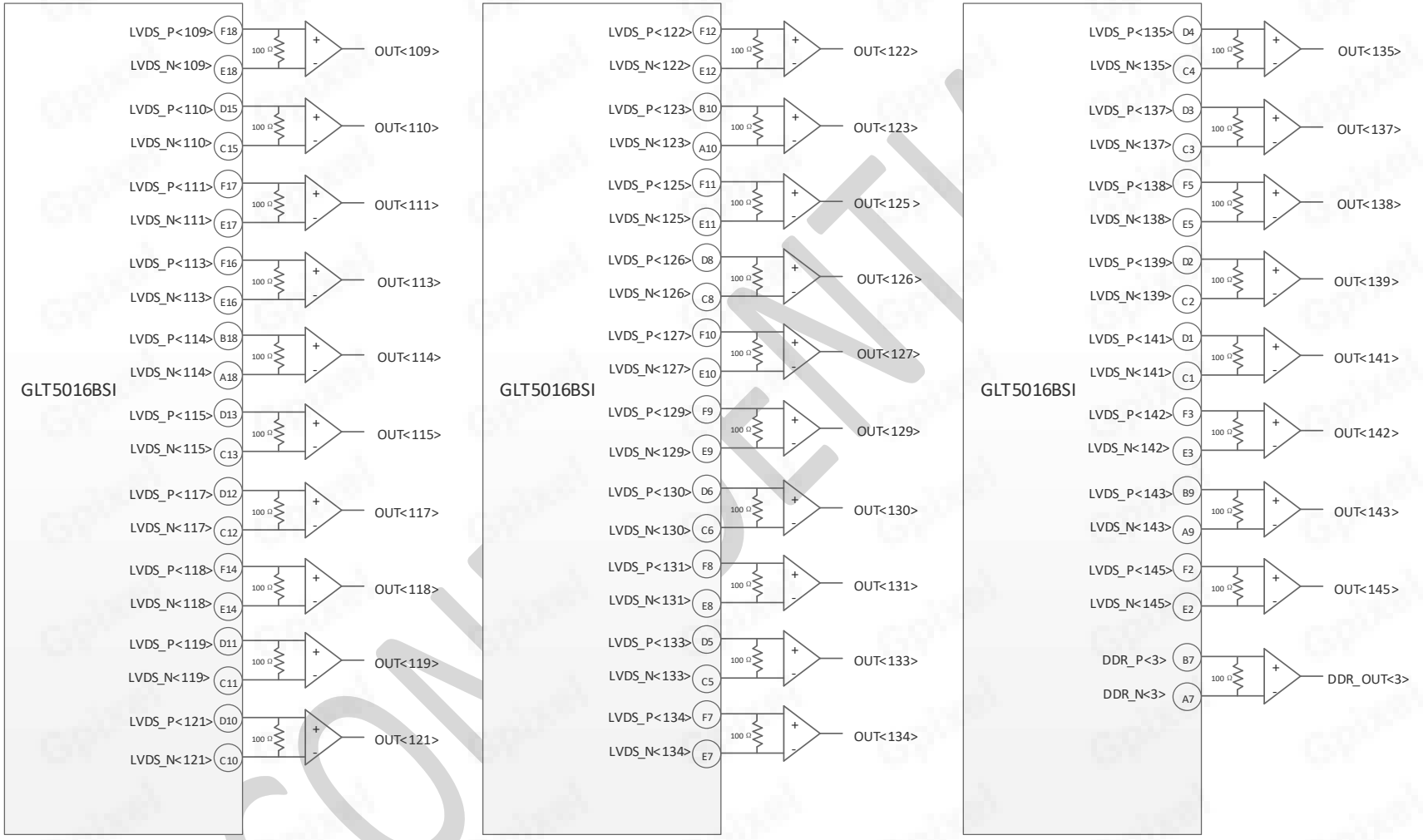


Figure 22 GLT5016BSI Sub-LVDS output connection

Power On/Off Sequence

The power supplies should follow the power on/off sequence as illustrated in Figure 23. To avoid current peaks during power on and off, minimum time delays should be guaranteed. The SPI configuration should include fourteen phases as illustrated in Figure 23 which are named SPI config1-SPI config14. Configuration in each phase should be:

- SPI config1: Write H<101> as 8'h8;
- SPI config2: Write all registers with recommended values depending on the working mode selected, except for the addresses shown in Table 13, which should be written with corresponding values in Table 13;
- SPI config3: Write the register in address H<101> as 8'h18;
- SPI config4: Write the register in address H<101> as 8'h1A;
- SPI config5: Write the register in address H<0> as 8'h1;
- SPI config6: Write the register in address H<101> as 8'h12;
- SPI config7: Write the register in address H<101> as 8'h1A;
- SPI config8: Write the register in address H<0> as 8'h0;
- SPI config9: Write the register in address H<0> as 8'h1;
- SPI config10: Write the register in address H<101> as 8'h18;
- SPI config11: Write the register in address H<101> as 8'h8;
- SPI config12: Write the register in address H<101> as 8'h18;
- SPI config13: Write the register in address H<101> as 8'h1A;
- SPI config14: Only write registers mentioned in Table 13 with recommended values depending on the working mode selected in Register Map.

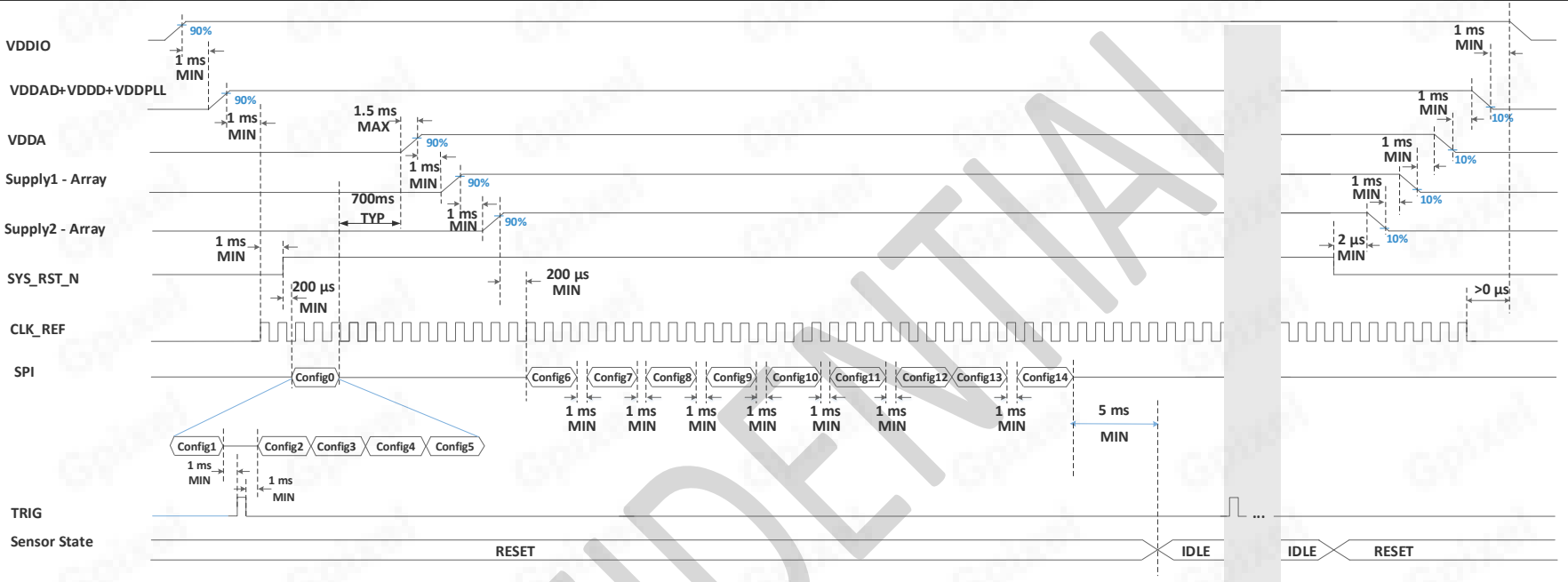


Figure 23 Power-on and power-off sequence

Table 13 Related addresses for SPI config2

Hex address	Hex value	Hex address	Hex value	Hex address	Hex value	Hex address	Hex value
80A	FF	80E	FF	811	7F	81B	FF
80B	7F	80F	FF	814	BA		
80C	7F	810	FF	819	FF		

NOTE:

1) CLK_STABLE_EN should always be 1 when the sensor is actively capturing images after power-on.
2) Supply2-array includes VAGL, VBGL, VTXL, VABG and VRSTL.
3) Except VDDAD, VDDD, VDDPLL, VDDA, VDDIO and 5 supplies in Supply2-Array, other supplies are defined as Supply1-Array.

4) Write register of config12 and config13 separately, not together. Moreover, write them continuously without any time interval.
5) The power-on establishment time of VDDA should be less than 1.5ms. (from 0% to 90%).
6) The typical time interval for config5 and VDDA to start powering on is 700ms. The range of the time intervals is 650ms to 750ms.

Sensor Configuration

All on-chip registers should be programmed to the recommended value as listed in the register map before image capture. This section lists some basic sensor configurations that user may want to change for specific applications. For more options, please refer to section 'Description of Various Functions'.

Reset Sequence

The sensor reset sequence is shown in Figure 24. All the signals in the figure should follow the corresponding minimal time delays for correct reset operation. All programming registers will be reset to their default value when SYS_RST_N is set to '0'. It is necessary to reconfigure the registers before image capture. If different CLK_PIX frequency is required while the sensor is running, the sensor reset sequence must be executed.

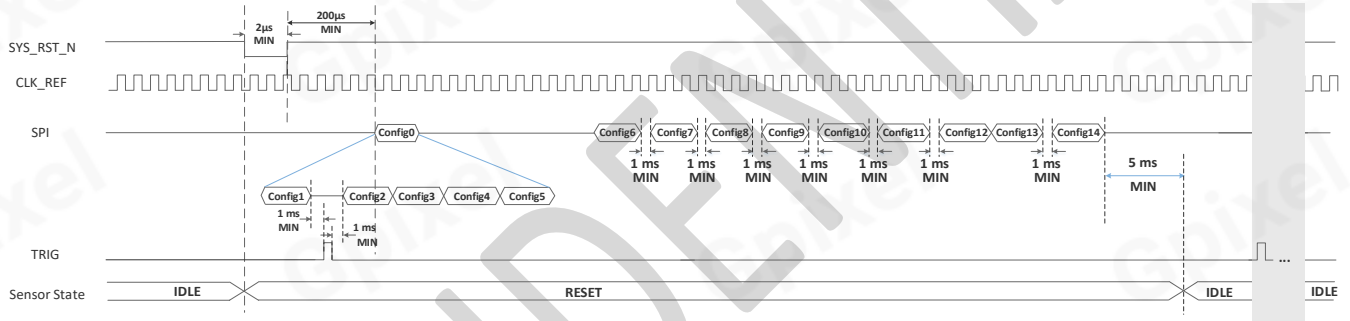


Figure 24 Sensor reset sequence

NOTE:

1) Write register of config1 ~ config14 in the same way as shown in Power On/Off Sequence.
2) Write register of config12 and config13 separately, not together. Moreover, write them continuously without any time interval.

Register Communication Timing

There are in total 329 bytes of registers in GLT5016BSI. After the sensor power on, all registers will be reset to default state. Some of the registers need to be re-configured before proper operation of the sensor. The read and write of these registers are through the SPI interface. Details about the read and write operation are explained below.

SPI WRITE

The data is sampled by the GLT5016BSI on the rising edge of SPI_CLK. SPI_CLK has a fixed frequency of 5MHz. SPI_CS_N signal has to be low for half a clock period before the first data-bit is sampled. SPI_CS_N has to remain

low for 1 clock period after the last data-bit is sampled. The sampled data will be written in the sequencer on the last falling clock edge, so SPI_CLK has to go low again at the end for the write operation to be successful.

One write action contains at least 24 data-bits:

- One control bit: The first bit to be sent, indicating whether the operation is write (‘1’) or read (‘0’).
- 15 address bits: These bits form the address of the programming register that needs to be written. The address is sent MSB first.
- 8 data bits: These bits form the actual data that will be written in the register selected with the address bits. The data is written MSB first.

It is also possible to write a consecutive of registers by sending more data-bits in one write operation. In this case only the first address of the registers need to be written. After the data writing of the first address N, the sensor will automatically write the following 8-bit data to address N+1. The timing diagram of the SPI write operation is shown in Figure 25.

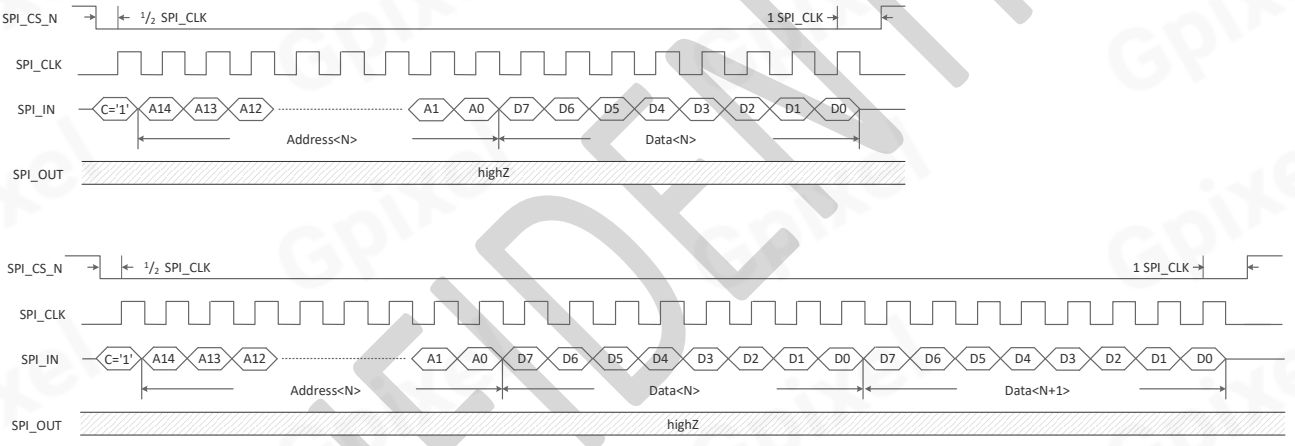


Figure 25 SPI write timing

SPI READ

The control bit on SPI_IN pin is set to ‘0’ in order to read the registers from the interface. The address of the register being read out is sent immediately after this control bit (MSB first). The data is sent out from SPI_OUT pin on the falling edge of SPI_CLK, with MSB first.

Like write operation, it is also possible to read a consecutive of registers by keeping SPI_CS_N low after readout of the first address. The timing diagram of the SPI read operation is shown in Figure 26.

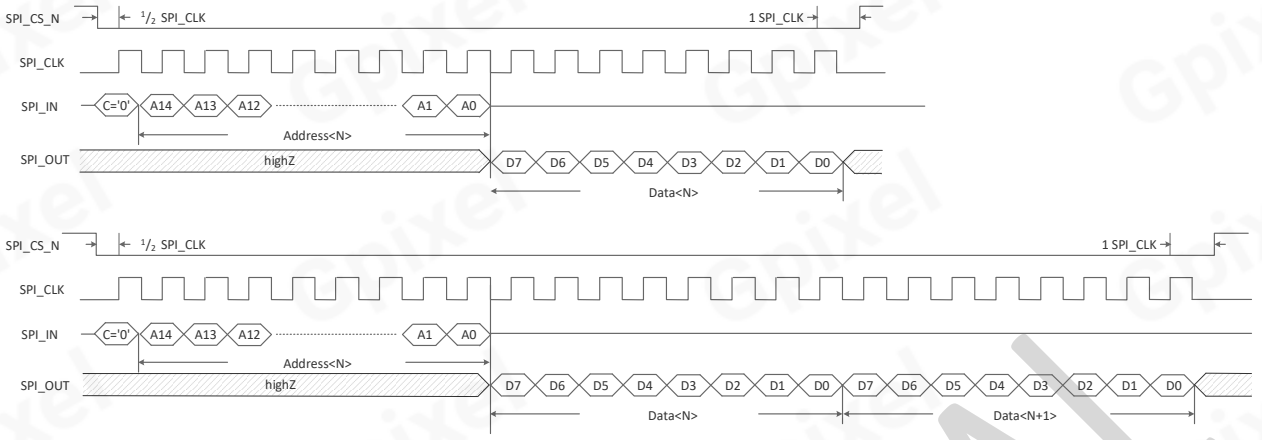


Figure 26 SPI read timing

Clock System

The clock system of GLT5016BSI is illustrated in Figure 27. An input clock (CLK_REF) with a fixed frequency of 40MHz for 10-bit mode and 80MHz for 12-bit mode is required to correctly operate the sensor.

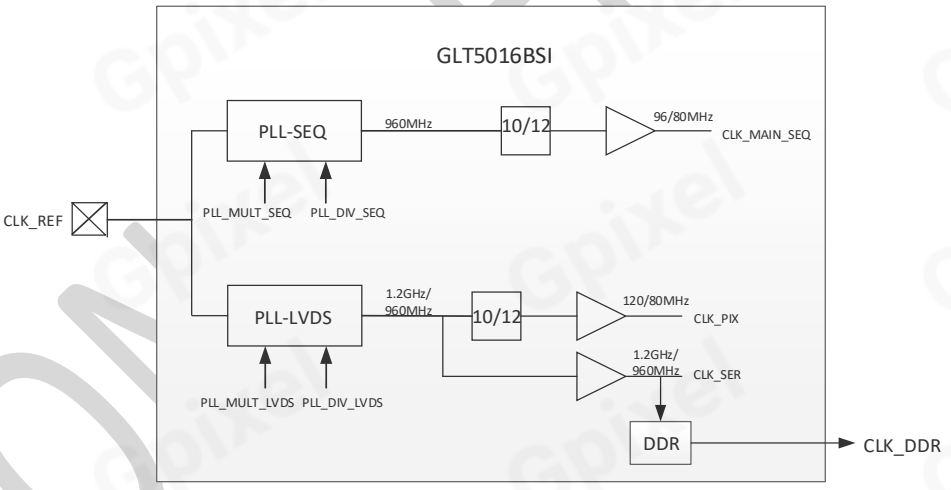


Figure 27 Internal clocking scheme

Table 14 Clock system in GLT5016BSI

Clock	Description
CLK_SER	Serial clock, used to serialize the pixel data before sending over the output channels
CLK_PIX	Parallel or pixel clock, determines pixel readout rate
CLK_MAIN_SEQ	Clocks used for on-chip timing generator (SEQ)

Two internal PLL is used to derive the required internal clock frequencies from input clock. The settings ‘pll_mult’ and ‘pll_div’, which can be programmed via the SPI registers, determine the internal clock frequencies.

The frequency of the internally generated high-speed clock CLK_SER can be calculated by the PLL multiplication factor (M_X) and PLL dividing factor (D_Y), as shown below:

$$F_{CLK\_SER} = F_{CLK\_REF} \times M_X / D_Y$$

Where $480MHz \leq F_{CLK\_REF} \times M_X \leq 1200MHz$. Details for PLL register settings are shown in Table 15.

Table 15 Registers for PLL setting

Address(Hex)	Bit	Name	Description
FF	2:1	PLL_DIV_SEQ<1:0>	SET PLL dividing factor Dy: 0: /1 1: /2 2: /4 3: /8
FF	0	PLL_MULT_SEQ<3:0>	SET PLL multiplication factor Mx: 0: prohibition M_X = PLL_MULT_SEQ x 2+2 Ex)1011: M_X=11*2+2=24
FE	7:5		
FD	7:6	PLL_DIV_LVDS<1:0>	SET PLL dividing factor Dy: 0: /1 1: /2 2: /4 3: /8
FE	4:1	PLL_MULT_LVDS<3:0>	SET PLL multiplication factor Mx: 0: prohibition M_X = PLL_MULT_LVDS x 2+2 Ex)1011: M_X=11*2+2=24

Trigger and Sensor Line Time

The time external between the rising edges of the Trigger signal (TRIG) is defined as the sensor line time.

The external trigger signal and sequencer internal state relation is shown in Figure 28. The sequencer output starts from Time0 until pre-set line-time (TimeX). During this period, no new TRIG is allowed. After the TimeX, the sequencer is in idle state, waiting for the next trigger.

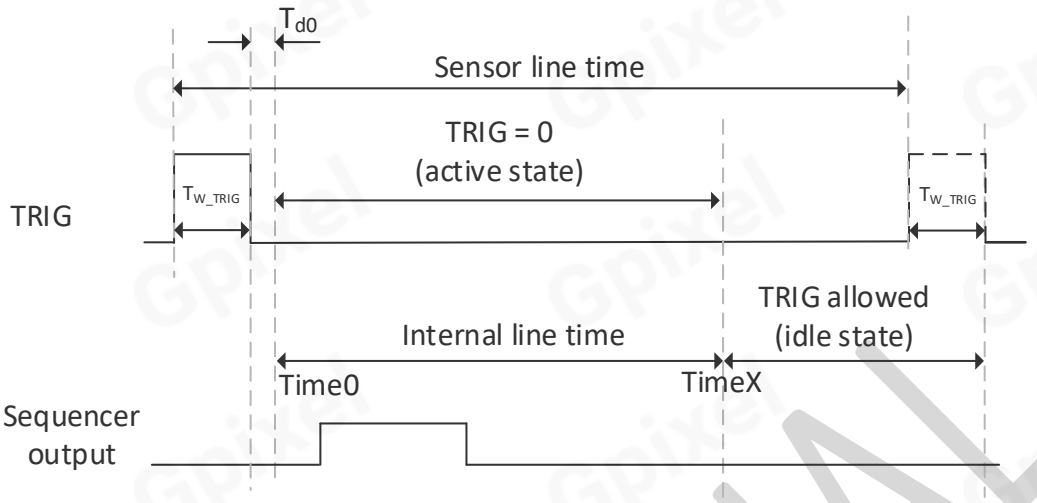


Figure 28 Trigger and Line time

NOTE:

1) T_{W_TRIG} is the pulse width of TRIG, equals to: $\frac{1}{CLK\_MAIN\_SEQ}$

2) T_{d0} is 4ns in typical case.

3) Suggested adjustment step for sensor line time in 12-bit mode is one cycle of CLK_REF ($\frac{1}{80MHz}$ for 12-bit mode), and no requirement for 10-bit mode.

Internal Line Time

LINE_U_LENGTH is used to determine the internal line time, LINE_U_LENGTH register listed in Table 16.

Table 16 Line length register

Address(Hex)	Bit	Register Name	Description	Default Value
B	7:0	LINE_U_LENGTH	Line time unit length.	16'd158@12bit 16'd101@10bit
A	7:0			

NOTE:

1) LINE_U_LENGTH is controlled by 16-bit registers, 8 MSB are from address B (HEX), low 8 bit from address A (HEX). For example, if 259 is the target setting, 8 MSB and 8 LSB are 1 and 3 in decimal (00000001 and 00000011 in binary).

The internal line time can be calculated as:

$$T_{INT\_LINE}=LINE\_U\_LENGTH\times T_{CLK\_MAIN\_SEQ}$$

Where $T_{CLK\_MAIN\_SEQ}$ is the period of CLK_MAIN_SEQ. For example, suppose LINE_U_LENGTH is set to 240, the Line time T_{INT_LINE} is 240 CLK_MAIN_SEQ cycles.

Line Rate Calculation

The line rate is the reciprocal of the line time.

The sensor line time can be referred to Trigger and Sensor Line Time.

Reading Out the Sensor

Sub-LVDS Output

GLT5016BSI uses Sub-LVDS outputs for image data read out. There are 110 sub-LVDS data channels LVDS<0:145>, and 4 clock channels DDR<0:3> in total.

The data channel is used to transport the image data to the receiving end of the surrounding system. The clock channel outputs a Double Data Rate (DDR) clock which can be used at the receiving end to sample the image data. It is synchronous to the data channels with minimum skew.

Clock Channels

The clock channel sends out a constantly running clock signal which is aligned to the data on the output channels. The data sampling clock must be derived from this clock signal. As data channels operate at Double Data Rate (DDR), data must be sampled on both clock edges. Please note, there are 27 data channels and one dedicated clock channel in each stitching cell and the output data in stitching cell must be sampled by the dedicated clock.

NOTE:

1) The DDR clock generated by DDR<0> is used for sampling the image data from LVDS<0:35>, DDR<1> is for LVDS<37:71>, and DDR<2> is for LVDS<73:107>, and DDR<3> is for LVDS<109:145>.

Data Interface Training

For correct data receiving, it is recommended to train the output data interface before image capture.

Described in section 'Sensor Setting Flow', a known training pattern (TP) will be output continuously on all data channels after CLK_STABLE_EN release to state '1'. The training pattern will be output while no image data is being transferred.

Registers detail with data interface training are shown in Table 17.

Table 17 Register setting for data interface training

Address(Hex)	Bit	Name	Description
106	3:0	Training Pattern <11:0>	Recommended training pattern is 12'h165.
105	7:0		

NOTE:

1) It is recommended to route the sub-LVDS output traces on PCB as similar as possible.

2) The serial data is sent out with LSB first.

3) The lower 10bit of training pattern (Training Pattern <9:0>) is used for 10-bit ADC mode, recommended training pattern is 10'h165.

Image Data Output Format

Once "TRIG" is pulsed and ADC operation is finished, the row data is transmitted over the data interface. This section describes how the image data is formatted.

Block Based Readout

Reading out the image data occurs in blocks as indicated in Figure 29. The green line is stitching line, and the M area between two stitching lines is the stitching cell. GLT5016BSI sensor contains 4 stitching cells. There is a data channel in left, a data channel in right and 27 data channels in each stitching cell.

Note that the leftmost and rightmost channels will send out data which contains both dark and dummy pixel data. The leftmost column is defined as the first column and the rightmost column is defined as the last column for the whole sensor.

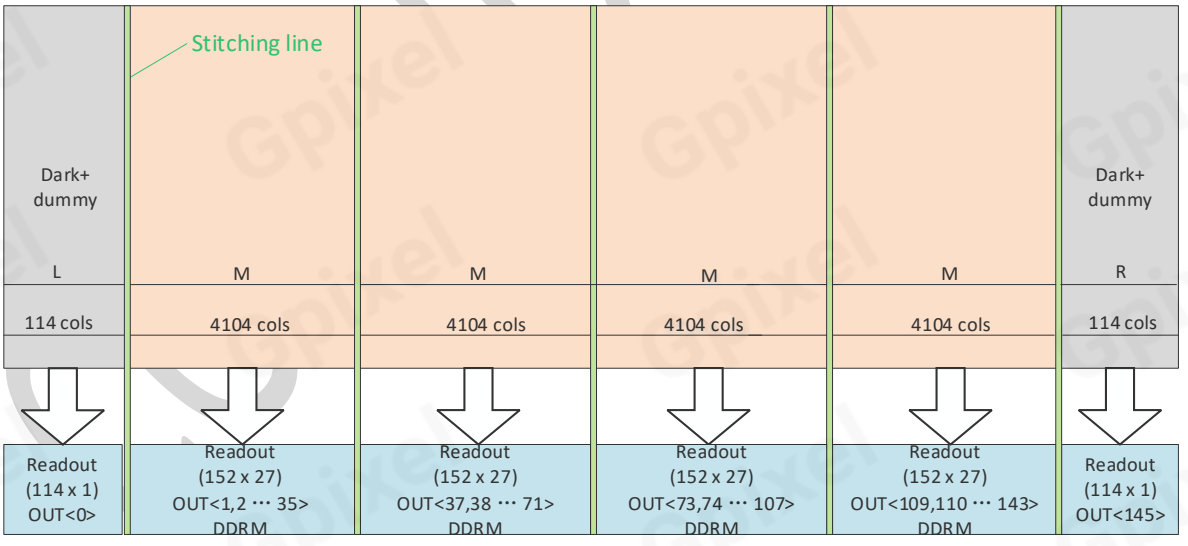


Figure 29 Block-based readout architecture

Channel Multiplexing

The sensor supports several channel multiplexing modes. In these modes, the image data is sent out over a limited number of output channels. The supported number of effective readout data channels are 108, 96, 72, 48, 36, 24,

12 for 12-bit mode, and 72, 48, 36, 24, 12 for 10-bit mode. Except for the effective readout channels, 4 DDR channels and 2 dark and dummy channels also need to be output for each mode.

Please refer to Figure 27 for maximal data rate at the outputs. It is noted that lowering the number of readout channels will also lower the line rate.

Figure 30 shows the details about the pixel mapping with channel multiplexing for effective image in one stitch region, that is the M region in Figure 29. The 2 OB output channels do not support channel multiplexing function. For each pixel output word, LSB output first.

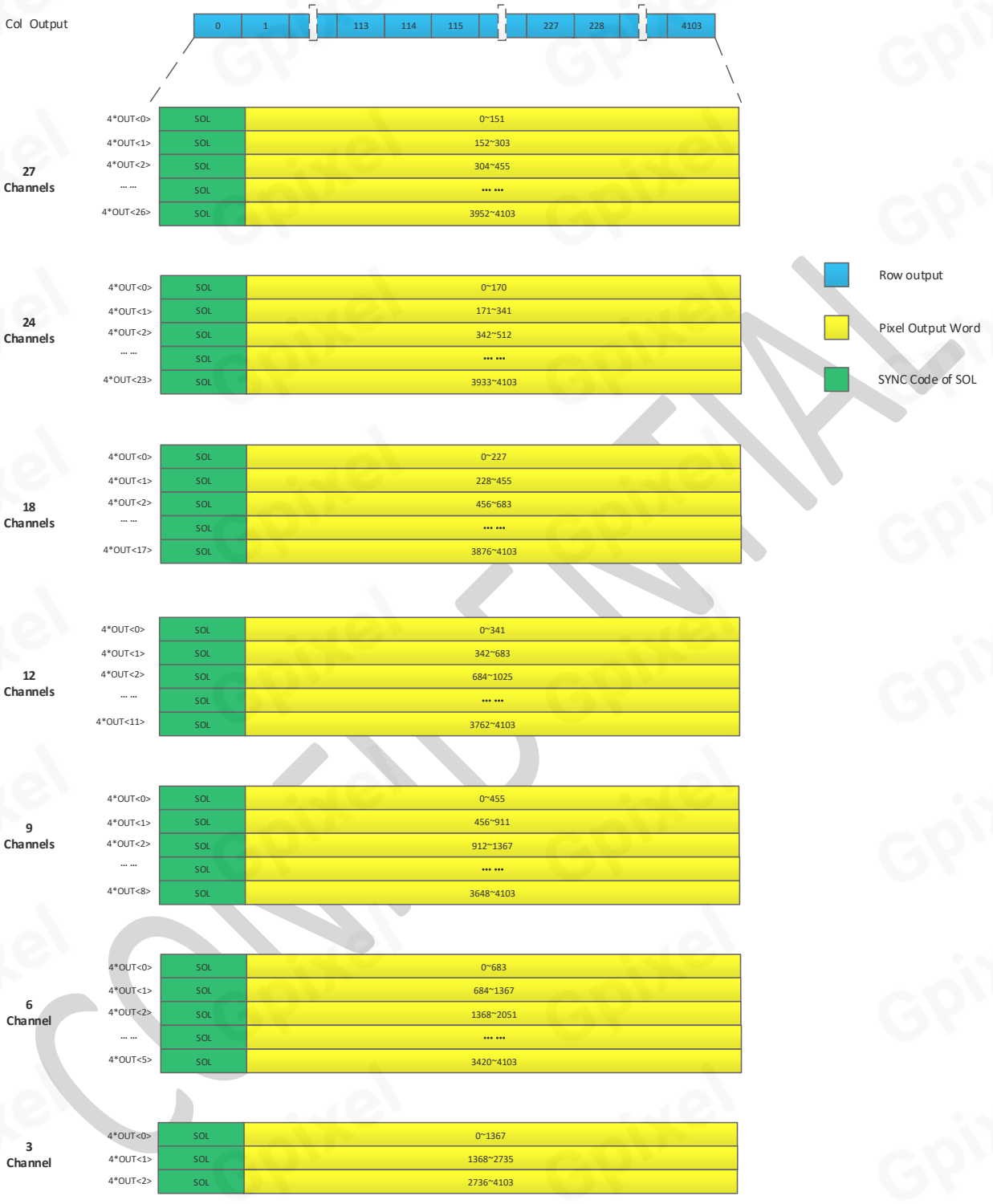


Figure 30 Pixel mapping with channel multiplexing

Table 18 illustrates the effective channels with multiplexing in different output modes.

Table 18 Output channel setting

Address(Hex)	Bit	Register	Value	Output Mode	Enable Channels
118	2:0	LVDS_MUX	7	12 channel output mode.	OUT<0>

					OUT<1,13,25,37,49,61,73,85,97,109,121,133> OUT<145>
			6	24 channel output mode.	OUT<0> OUT<1,7,13,19,25,31,37,43,49,55,61,67,73,79,85,91,97,103,109,115,121,127,133,139> OUT<145>
			5	36 channel output mode.	OUT<0> OUT<1,5,9,13,17,21,25,29,33,37,41,45,49,53,57,61,65,69,73,77,81,85,89,93,97,101,105,109,113,117,121,125,129,133,137,141> OUT<145>
			4	48 channel output mode.	OUT<0> OUT<1,4,7,10,13,16,19,22,25,28,31,34,37,40,43,46,49,52,55,58,61,64,67,70,73,76,79,82,85,88,91,94,97,100,103,106,109,112,115,118,121,124,127,130,133,136,139,142> OUT<145>
			3	72 channel output mode.	OUT<0> OUT<1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63,65,67,69,71,73,75,77,79,81,83,85,87,89,91,93,95,97,99,101,103,105,107,109,111,113,115,117,119,121,123,125,127,129,131,133,135,137,139,141,143> OUT<145>
			2	96 channel output mode.	OUT<0> OUT<1,2,4,5,7,8,10,11,13,14,16,17,19,20,22,23,25,26,28,29,31,32,34,35,37,38,40,41,43,44,46,47,49,50,52,53,55,56,58,59,61,62,64,65,67,68,70,71,73,74,76,77,79,80,82,83,85,86,88,89,91,92,94,95,97,98,100,101,103,104,106,107,109,110,112,113,115,116,118,119,121,122,124,125,127,128,130,131,133,134,136,137,139,140,142,143> OUT<145>
			1	108 channel output mode.	OUT<0> OUT<1,2,3,5,6,7,9,10,11,13,14,15,17,18,19,21,22,23,25,26,27,29,30,31,33,34,35,37,38,39,41,42,43,45,46,47,49,50,51,53,54,55,57,58,59,61,62,63,65,66,67,69,70,71,73,74,75,77,78,79,81,82,83,85,86,87,89,90,91,93,94,95,97,98,99,101,102,103,105,106,107,109,

					110,111,113,114,115,117,118,119,121,122 ,123,125,126,127,129,130,131,133,134,13 5,137,138,139,141,142,143> OUT<145>

Using the channel multiplexing function requires synchronized adjustment of the sensor line rate. The following table shows the channel output mode and minimum sensor line time.

Table 19 Minimum sensor line time under each channel output mode

Channel output mode	Pixel data per channel	Minimum sensor line time/μs	
		10bit	12bit
12 channel output mode.	1368	11.5500	17.3250
24 channel output mode.	684	5.8417	8.7625
36 channel output mode.	456	3.9333	5.9000
48 channel output mode.	342	2.9750	4.4625
72 channel output mode.	228	1.9917	3.0125
96 channel output mode.	171	-	2.2750
108 channel output mode.	152	-	1.9875

Line Format

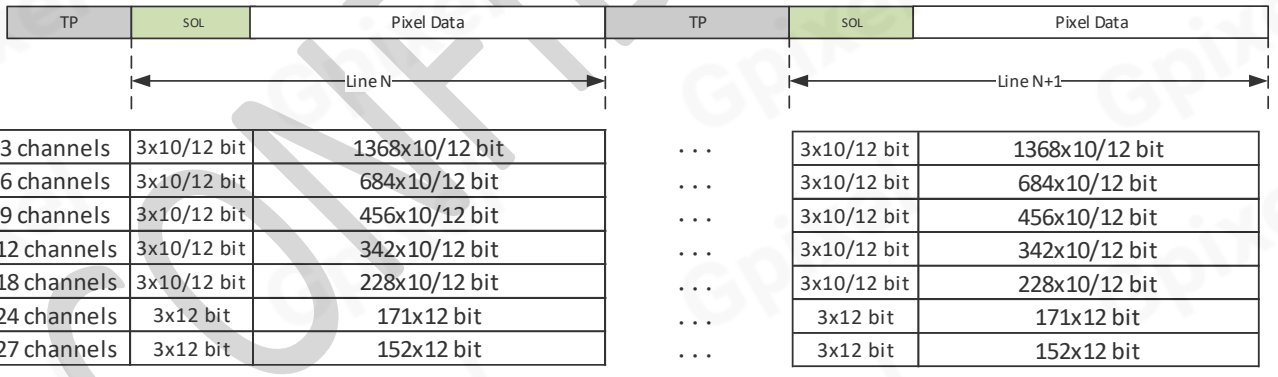


Figure 31 Line format

GLT5016BSI supports 10-bit and 12-bit ADC output. Figure 31 graphically represents the line data format in the stitch region. Please refer to Channel Multiplexing for channels of 10-bit and 12-bit mode.

A single line period outputs all the column pixel data. The data of multiple output channels are shown in the table in Figure 31.

- If no image readout is ongoing, the Training Pattern (TP) is sent out.

- Image data always start after 'Start' synchronization (SYNC) codes. Each of such SYNC code consists of 3/4 words which is shown in Figure 34 (Single band mode: 3words. Dual band mode: 4words).
- Table 20 shows the SYNC code details. These codes can by design never occur in an image data stream, as in the image data stream the code 000h will not be present.
- The start of the first column of a line is indicated by a 'Start of Line' (SOL) SYNC code.
- In order to distinguish the pixel data output from the Pixel Array1 or the Pixel Array2, two sets of sync codes are defined in SYNC Code.

The length of the pixel data period in each line is dependent on the selected channel multiplexing mode. To achieve maximum line rate, 108 available channels in 4M regions in Figure 29 are output for 12bit, and 72 available channels are output for 10bit. For each output channel in M region, 152x12bit and 228x10bit are output separately for 12bit and 10bit.

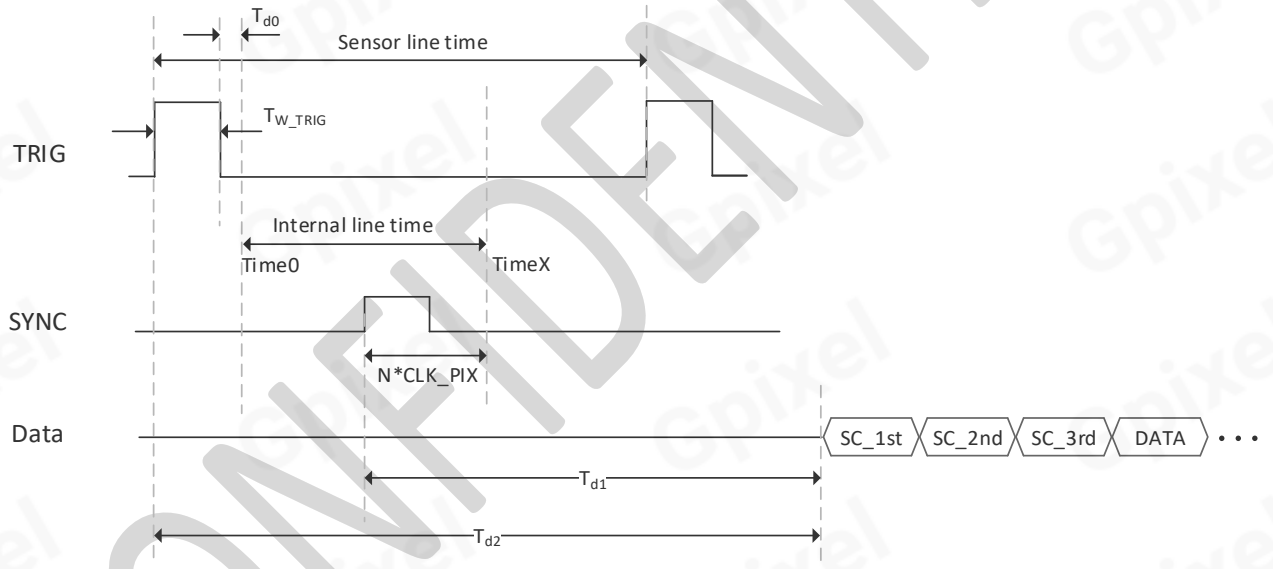


Figure 32 Data reception process

Data reception process of GLT5016BSI is shown in Figure 32, in which T_{d1} and T_{d2} can be calculated as:

$$T_{d1}=54*CLK\_PIX$$

$$T_{d2}=T_{W\_TRIG}+T_{d0}+(LINE\_U\_LENGTH-N)*CLK\_PIX+T_{d1}$$

The default pulse width of SYNC (sync_length) is 2*CLK_PIX, and the default value of N is 44@10bit and 51@12bit (N should be more than sync_length +1). N can be set in register. TW_TRIG is pulse width of TRIG, its value can be referred to Trigger and Sensor Line Time. T_{d0} can be referred to Trigger and Sensor Line Time.

As shown in the figure below, the pixel data is output with a delay of 1*Sensor line time plus T_{d2}.

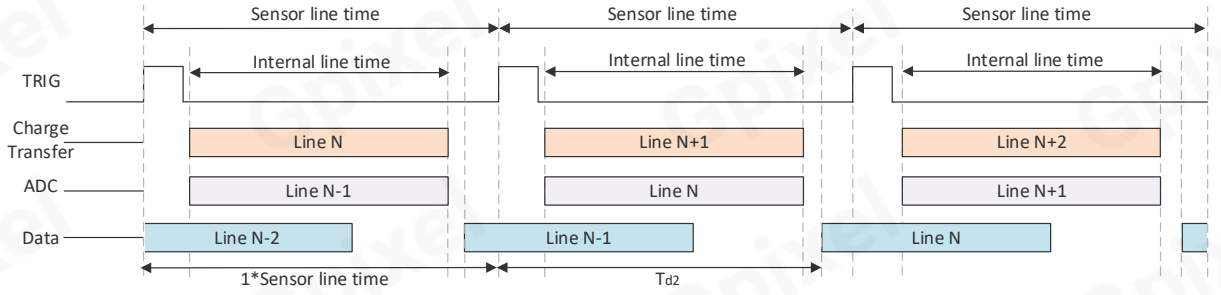


Figure 33 Trigger and valid data output

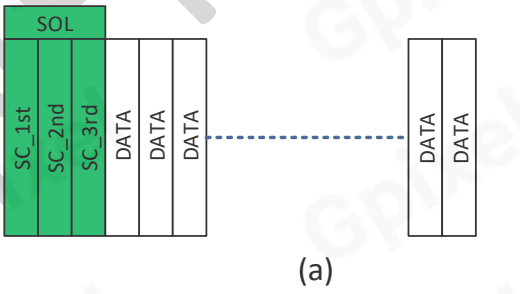
SYNC Code

Sync code is added in the image sensor output to indicate the correct pixel data. There are four types of Sync codes used in GLT5016BSI sensor. They are listed below in Table 20 .

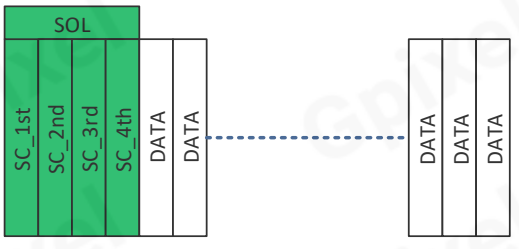
Table 20 Sync code in different bit modes

Band	Mode	SC_1st	SC_2nd	SC_3rd	SC_4th
P1	10bit	10’ h3FF	10’ h000	10’ h000	10’ h2AC
	12bit	12’ hFFF	12’ h000	12’ h000	12’ hAB0
P2	10bit	10’ h3FF	10’ h000	10’ h000	10’ h2AD
	12bit	12’ hFFF	12’ h000	12’ h000	12’ hAB4

Figure 34 illustrates the image data output format for GLT5016BSI sensor. TP code is data word based and placed any moment when SYNC code and valid data are not output.



(a)



(b)

Figure 34 GLT5016BSI image data output

NOTE:

1) In single band mode, data output starts with three SYNC code shown in figure(a) in Figure 34, and in dual band mode, data output starts with four SYNC code shown in figure(b) in Figure 34.

Sensor Settling Time

GLT5016BSI outputs all the rows information accompanying the trigger signals. The first rows equaling to the TDI stage selection is the establishment process of TDI, this information is not usable.

Based on the current peripheral circuit design in the datasheet, some analog bias needs more stability time compared to the TDI establishment process. Generally, 700 rows should be waited to get the stable image for 10-bit and 12-bit mode.

Description of Various Functions

Analog Gain

GLT5016BSI supports analog gain of 1x to 4x with step of 1 for 12-bit mode, analog gain of 1x and 2x for 10-bit mode. Table 21 describes the register for 12-bit analog gain setting. Table 22 describes the register for 10-bit analog gain setting.

Table 21 Registers for analog gain setting in GLT5016BSI 12bit 500kHz

Address(Hex)	bit	Register name	Setting(Hex)			
			1x	2x	3x	4x
814	5:4	ANA_GAIN	1	2	1	0
819	5:0		26	A	A	24
10B	6:0		6C	50	50	70
10C	1:0		0	1	1	1
11B	0		0	0	0	0
10F	0		0	0	0	0
112	5:0		1B3	185	181	174
111	7:0					

Table 22 Registers for analog gain setting in GLT5016BSI 10bit 500kHz

Address(Hex)	bit	Register name	Setting(Hex)	
			1x	2x
814	5:4	ANA_GAIN	2	0
819	5:0		19	35
10B	6:0		0	0
10C	1:0		0	0
11B	0		1	1
10F	0		1	1
112	5:0		78	A5
111	7:0			

NOTE:

1) When using 2x gain in 10-bit mode, the dark offset needs to be increased synchronously. Refer to Table 22 for the specific setting values.

Pixel Band Selection

Table 23 shows the pixel band selection register configuration.

Table 23 pixel band selection setting

Address(Hex)	bit	Register name	Description
1	0	REG_P1_EN	1: Pixel array1 enable 0: Pixel array1 disable
2	0	REG_P2_EN	1: Pixel array2 enable 0: Pixel array2 disable

Area Mode

The sensor can be operated in Area Mode, and the horizontal resolution is 16644. When operating in Area mode, the height feature changes to 256 with P1 band TDI selecting 256 stages or 32 with P2 band TDI selecting 32 stages automatically. The height features various with the TDI stage selection, and the TDI stages selections refers to Table 25 and Table 26 .

The sensor trigger signal (TRIG) trigged the sensor internal timing by each line time at TDI mode. While in the Area mode, the TRIG should be stopped X line times to make the pixel exposure (X is a positive integer), and then trig sensor at each line time to readout the pixel array in TDI mode. During the Area readout time, the light should be turned off. Figure 35 shows the working diagram of Area mode with N rows.

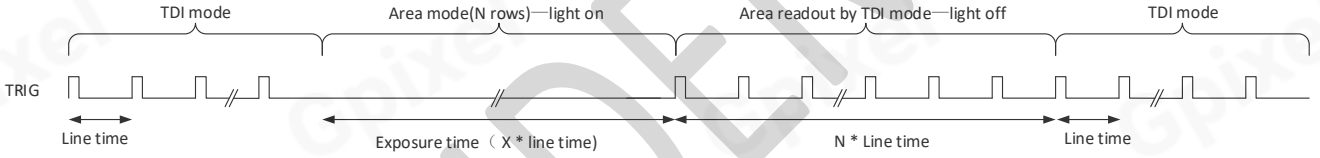


Figure 35 Area mode working timing

TDI Pushing Scan Direction

GLT5016BSI supports both reverse TDI pushing scan and forward TDI pushing scan. In Figure 36 and Figure 37, the arrow direction indicates the object movement direction relative to the sensor. If objects move down, forward scanning is defined as shown in Figure 36; if the objects move up, which is defined as reverse scanning in Figure 37.

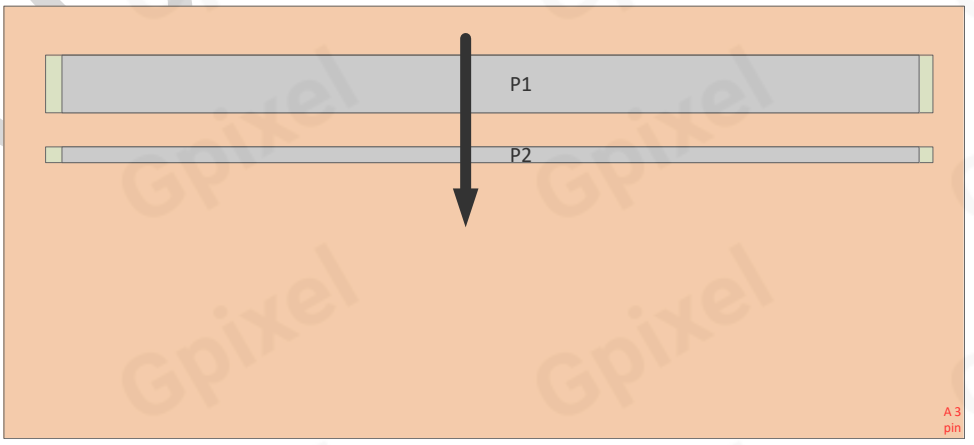


Figure 36 forward scanning definition

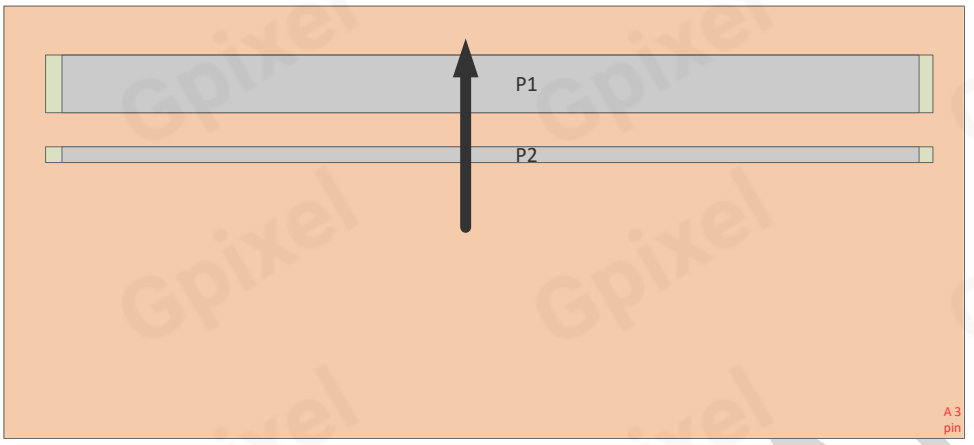


Figure 37 reverse scanning definition

Table 24 shows the SPI configuration for the TDI scanning direction.

Table 24: Pixel scanning direction setting

Address(Hex)	Bit	Register name	Forward scanning setting	Reverse scanning setting
6	0	REG_TDI_TOP_SCAN_EN	0	1

TDI Stage Selection

GLT5016BSI supports various TDI stage selections. The maximum TDI stage of P1 and P2 are 256 and 32, and the TDI stage selection is controlled by the different SPI. The table below show the TDI stage selections for both forward and reverse TDI direction.

Table 25: TDI stage selection of P1

Address(Hex)	Bit	Register name	Register setting (MSB to LSB)	TDI stage(5μm) Reverse TDI & Forward TDI
7	3:0	REG_P1_STAGE	0000	--
			0001	4
			0010	32
			0011	64
			0100	128
			0101	192
			0110	224
			0111	252
			1000	256

Table 26: TDI stage selection of P2

Address(Hex)	Bit	Register name	Register setting (MSB to LSB)	TDI stage(5μm) Reverse TDI& Forward TDI
8	3:0	REG_P2_STAGE	0000	--
			0001	2
			0010	4
			0011	8
			0100	16
			0101	24
			0110	28
			0111	30
			1000	32

Black Level

The black level for readout can be set by register. The register is 14-bit complement integer. The black level offset changes linearly with this number. Dark offset of P1/P2 can be configured independently.

Table 27 Registers for dark offset setting of GLT5016BSI

Address(Hex)	Bit	Name	Description
114	5:0	DOFF_P2	Dark offset for pixel array2.
113	7:0		
112	5:0	DOFF_P1	Dark offset for pixel array1.
111	7:0		

NOTE:

1) The black level changes with different temperatures and sensor samples with default register setting. Users are recommended to fine tune the above registers per sensor, according to the output dark image level.

Image Flipping

GLT5016BSI supports image flipping horizontally in each channel, and customer needs to flip the available channels off chip. Figure 38 shows the flipping image. Please note that when register FLIP_EN as listed in Table 28 is enabled, the pixel mapping needs to be adapted (or more specifically, flipped) as well. OB data output only flip within the channel respectively. Figure 39 and Figure 40 give examples of GLT5016BSI pixel mapping when FLIP_EN is enabled for 12bit and 10bit.

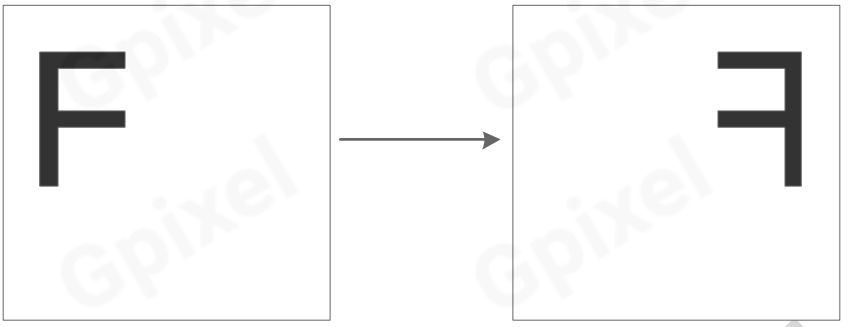


Figure 38 Image horizontal flipping

Table 28 Registers for image flipping

Address(Hex)	Bit	Name	Description
107	0	FLIP_H	0: Disable image flipping 1: Enable image flipping

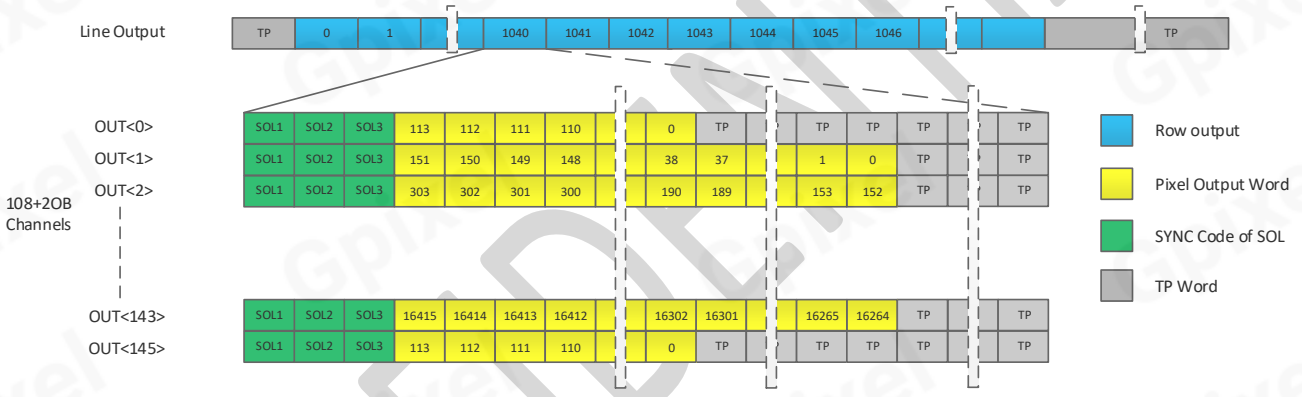


Figure 39 GLT5016BSI pixel mapping when flipping in enabled for 12bit

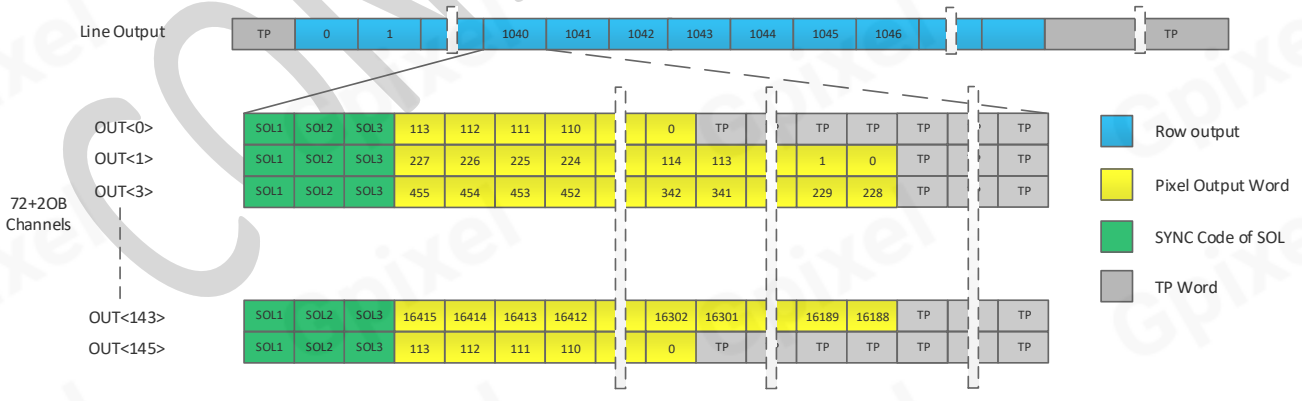


Figure 40 GLT5016BSI pixel mapping when flipping in enabled for 10bit

Test Image

GLT5016BSI can be configured to output a test image for users to debug the surrounding system. For example, excluding the repeating cells, it is a gradient image which have pixel values 1,1,2,3,⋯, 2^N-3,2^N-2,2^N-1(N means bit mode) starting from the left column when TEST_IMG_MODE is set to 1. Because all stitching regions consist 16416 columns, that means the test image pattern will repeat from 1 to 4095 with 12bit image data; repeat from 1 to 1023 with 10bit image data. The related registers to configure GLT5016BSI are described in Table 29. The test image is shown in Figure 41.

Table 29 Registers setting for GLT5016BSI to output test image

Address(Hex)	Bit	Name	Description
110	1:0	TEST_IMG_MODE	0: Normal pixel data 1: Column gradient test image output 2: Row gradient test image output 3: Diagonal gradient test image output

Figure 41 Column gradient test image output at 10bit mode

Temperature Readout

Analog Temperature Sensor

GLT5016BSI integrates analog temperature diode on chip. Its location on chip is shown in Figure 3.

Users should read analog temperature diode data after the chip is powered on. Recommended connections of this diode on board are shown in Figure 20. Please calibrate this temperature diode before using the sensor.

Digital Temperature Sensor

GLT5016BSI has an on-chip digital temperature sensor. The readout of this temperature sensor is through register TEMP_DATA_LSB(H<81E>) and TEMP_DATA_MSB(H<81F>). An example for the output of this temperature sensor (DN) versus the chip temperature is shown in the graphs below. The temperature of the sensor is usually obtained by using this fit line.

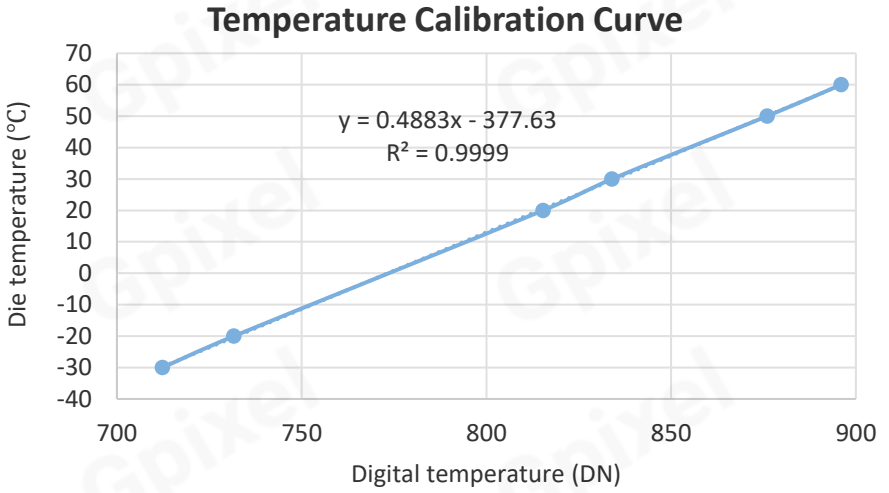


Figure 42 Temperature sensor for P1 10-bit mode

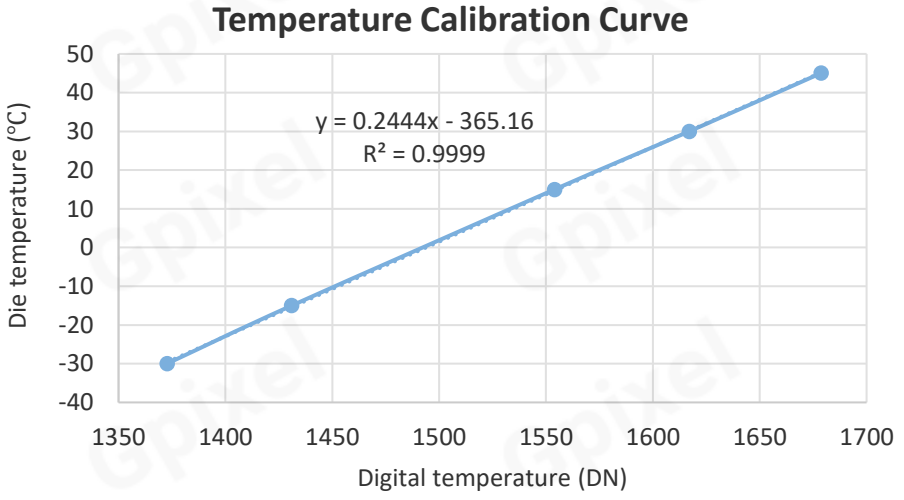


Figure 43 Temperature sensor for P1 12-bit mode

Note:

1) Please do individual characterization of the temperature sensor on each sensor for best accuracy.
2) The curve has high correlation with CLK_REF frequency of PLL(40MHz at P1 10-bit mode and 80MHz at P1 12-bit mode), when a change of CLK_REF happens, this curve needs to be re-characterized.

OTP Memory Readout

Reading out the OTP memory data occurs via the SPI interface. Figure 44 shows the single readout timing to read out the OTP memory.

- OTP Readout is initiated by writing the desired OTP address to SPI address 1401(hex).
- Next, reading address 1402(hex) sends out the data on the programmed OTP address of the SPI register.
- To jump to another OTP address, a new OTP address has to be uploaded to SPI address 1401(hex).

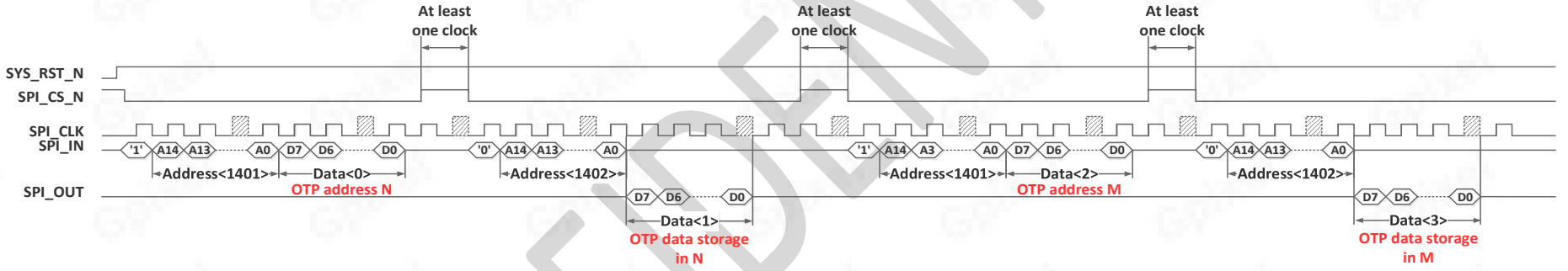


Figure 44 Single readout of OTP data

It is also possible to sequential readout the memory data. Figure 45 shows the operation timing.

- OTP Readout is initiated by writing the desired OTP address to SPI address 1401(hex).
- Next, reading address 1402(hex) sends out the data on the programmed OTP address of the SPI register.
- The following read of address 1402(hex) returns the following byte, etc.

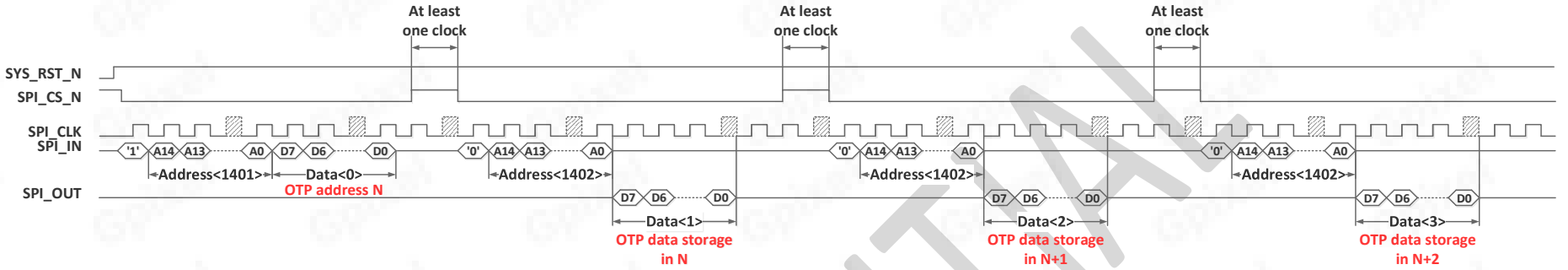


Figure 45 Sequential readout of OTP data

Note:

1) For example, the OTP data addresses 0, 1, 2 correspond to storing data of <7:0>, <15:8>, <23:16> bit respectively.

OTP Data Description

Bit address (DEC)	Bit width	OTP MAP name	Description	Example	OTP MAP data (HEX value, 'x' stands for any data)	
					<491:487>	<486:482>
<491:482>	10	Family name	It stands for product serial.	GLT	0	4
				GLT	4	x

Bit address (DEC)	Bit width	OTP MAP name	Description	Example	OTP MAP data (HEX value, 'x' stands for any data)	
					<237:222>	<221:206>
<237:206>	32	Sensor name	It should be decoded to DEC number. The family name is excluded.	5016BSI	0	1398
				5016BSI	1398	x

Bit address (DEC)	Bit width	OTP MAP name	Description	Example	OTP MAP data (HEX value, 'x' stands for any data)			
					<139:124>	<123:108>	<107:92>	<91:76>
<139:76>	64	Sensor variation	The sensor type variation should be decoded by ASCII code.	A5LV	0	0	564C	3541
				A5LV	564C	3541	x	x

				A5LU	0	0	554C	3541
				A5LU	554C	3541	x	x

Bit address (DEC)	Bit width	OTP MAP name	Description	Example	OTP MAP data (HEX value, 'x' stands for any data)			
					<75:60>	<59:44>		
<75:44>	32	Sensor lot number	It should be YYABB format which can be referred to the look-up-table.	YYABB = 23104	0	5C44		
				YYABB = 23104	5C44	x		

Bit address (DEC)	Bit width	OTP MAP name	Description	Example	OTP MAP data (HEX value, 'x' stands for any data)			
					<39:27>	<26:14>		
<39:14>	26	Sensor serial number	The serial number should be decoded to DEC number.	S/N = 0095	0	5F		
				S/N = 0095	5F	x		

Blemish Specification

GLT5016BSI sensor has 2 speed configurations: Median speed version and Normal speed version. The sensor outgoing test will be performed with the following configuration.

Table 30 Sensor configuration

Sensor speed version	Test mode	Test band	Pixel size	Test TDI stages
Median speed version	10bit single band	P1	5μm	4/128/256 stage
Normal speed version	12bit single band	P1	5μm	4/128/256 stage

Defect limits only apply to P1 effective pixel array of 16416 col x 256 stage that defined by below.

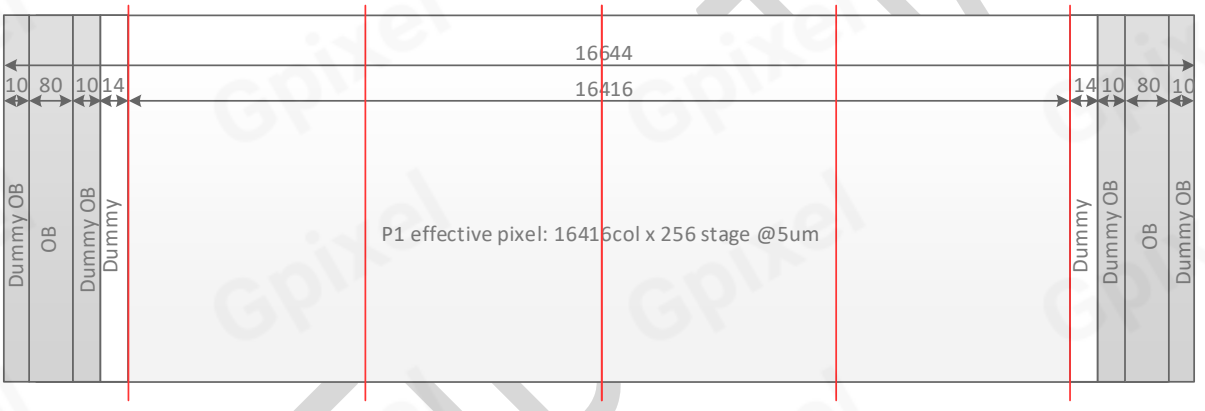


Figure 46 Defects controlled pixel array

Test Images

Test images as listed in Table 31 are grabbed with GLT5016BSI final tester at room temperature, under the illumination of a light source with uniformity better than 96% across the image area. These images are used for defect definitions. No image correction algorithm is applied.

Table 31 Test image definition

Image Level	Definition
Dark	100 line frames at fastest frequency in dark environment; the pixel average is performed on these frames to form the test image for the test TDI stages.
Grey	100 line frames at typical line frequency (f) to reach half-saturation in light environment; the pixel average is performed on these frames to form the test image for the test TDI stages.
Saturation	100 line frames at a line frequency of f/2 in light environment; the pixel average is performed on these frames to form the test image for the test TDI stages.

Defect Definitions

Table 32 below describes the definition of defects.

Table 32 Defect definition

Defect Name	Detail
Defect pixel in Dark image	Any pixel deviates more than 3% of the full swing(1) from the mean value of the Dark image.
Defect pixel in Grey image	Any pixel deviates more than 20% from the mean value of the Grey image.
Defect pixel in Saturation image	Any pixel deviates more than 20% from the mean value of the Saturation image.
Total defect pixels	The total number of non-overlapping bad pixels in Dark, Grey and Saturation image of all 3 stages.

Note:

1) Swing is equal to the difference between the mean value of the Saturation image and the mean value of the Dark image.

Defect Limits

Maximum allowed defect numbers are indicated below.

Table 33 Defect limits

Grade	Sensor speed version	Sensor mode	Defect Limits
Demo	Median speed version	10bit single band	No defect pixel
	Normal speed version	12bit single band	No defect pixel

Storage Condition and Handling

Handling Guideline

CMOS image sensors require delicate handling, ESD can cause sensor malfunction or even damages; many external elements, like dust, oil and scratches etc., can contaminate sensor glass lid and degrade sensor's performance. To reduce the risk of sensor damages, here Gpixel presents general guidelines and basic techniques for CMOS image sensor proper handling. Evidence of incorrect handling will invalidate the sensor warranty.

ESD Damage Prevention

To prevent ESD damage, Gpixel recommends following general procedures:

1. Ensure the ESD protective working area is properly set up.
2. Make sure the operator is grounded prior to handling the sensors.
3. Use ESD safe gloves to handle sensors.
4. Ground all tools and mechanical components that come in contact with the sensors.
5. Gpixel also recommends using antistatic solutions and air ionizers to prevent static charge buildup.

Protecting Sensor Glass Lid

The packaging of the CMOS sensors requires a high level of cleanliness. High quality glass lids, typically with anti-reflective coating, are part of the optical path and should be handled like other optical components with extreme care.

1. Perform the assembly in a clean environment (Class 10000 or better) to minimize the chance of dust contamination.
2. Wear mouth protection (face mask) to minimize the risk of contamination of glass lid.
3. Glove tips should be tight to reduce the risk of contaminating the glass lid.
4. Never touch the glass lid, especially the region over the photosensitive area.
5. Avoid making any contact with the glass lid with any object, especially hard objects to avoid scratches.

Gpixel recommends that all handling and assembly processes be audited and modified to reduce the risk of exposure to particles or contamination.

Glass Lid Cleaning

When particles and contaminants cannot be totally eliminated, it may be necessary to clean the glass cover lid. The procedure should be strictly followed to mitigate the possibility of glass lid damage.

1. Use clean compressed Nitrogen to blow off loose particles. Do not blow toward other parts. If you work under a flow box, try to blow out of box. This step alone is usually sufficient to clean the sensor window if the sensor is handled properly.
2. If further cleaning is required, use a lens wiper moistened with high-grade IPA.
3. Be cautious about cleaning agents, using agents other than IPA may result in attacking the glass lid attaching epoxy and degrading the reliability of the package.
4. Use lint-free ESD-safe cloth wipers that do not contain particles that can scratch the window. Do not use regular cotton swabs, since they can introduce charge to the window surface.
5. Wipe the window carefully and slowly until it covers the whole cleaning area. For line scan sensors, it may be easier to wipe along the width instead of the length.
6. Examine the cleaning result before attempting another cleaning procedure. If the surface cannot be cleaned after two or three wipes, it is possible that the stains or defects are the result of cover glass lid's permanent damage. Please inspect the glass lid under an optical microscope for signs of permanent damage.

Besides high-grade IPA, Gpixel recommends **First Contact Polymer Solutions** from **Photonic Cleaning** for cleaning of the lids.

Removal of Sensor Glass Lid

Removing the glass lid shall be treated with extreme caution. The following precautions are recommended in the glass-lid-removal procedure:

1. Work at a clean bench with HEPA filtered laminar air flow with Class 100 or better to minimize the airborne contamination;
2. Operator must wear a grounded wrist strap, antistatic cleanroom standard gloves, face masks, and head covers and should not wear cosmetics which contain damaging particles;
3. Once the lid is removed, the sensor must be stored and assembled in an environment as clean as possible, to avoid contamination;

In case particles fall in the photo-sensitive area, try to blow the dust or contamination away with a rubber squeeze dust blower. Do not remove the particles or dust with a swab or wipe, because the photo-sensitive area of the BSI sensors is vulnerable to stress, excess stress may induce higher dark current locally.

Note: Incoming test shall be conducted with taped glass lid NOT removed, as removing the glass lid will void the sensor warranty on certain claims, including but not limited to dust, scratch, bonding wire disconnection with pad etc.

Storage Condition

It is very important to minimize the contact of un-soldered sensor with moisture. We recommend the following storage conditions:

1. Open the sealed moisture barrier bag ONLY before assembly;
2. Re-seal the moisture barrier bag with desiccant for un-used sensors;
3. In case of IQC, the inspection should be carried out in a humidity controlled environment in minimal time, and the sensors should be re-sealed with desiccant after inspection.

Soldering Guideline

Gpixel recommends using sockets for BSI sensors camera assembly. If socket is not applicable, manual soldering can be used. The BSI sensors may be damaged in reflow soldering or wave soldering process.
When a soldering iron is used for manually soldering the sensors to a through-hole board, conditions as follows should be followed:

Profile Feature	Recommended Condition
Solder iron tip temperature	Max 350 ^{o}C
Pin temperature	Max 245 ^{o}C
Time	typical 2-3s, max 3 seconds

Please avoid global heating on ceramic packages during soldering.

Note: Gpixel recommends customers to purchasing engineering samples or mechanical samples to setup a suitable soldering process prior to applying the soldering process for mass production. The soldering profiles Gpixel provides are only for reference. Gpixel does not take responsibility if the sensor is damaged in the soldering processes.

Product Ordering Information

Product number	Grade	Description	Marking Code
GLT5016BSI-ABM-NUN-BUD	Demo	415-pin µPGA package. VIS version.12bit,500kHz,108pairs@960M. Sealed D263® Teco glass lid with AR coating on both sides.	GLT5016BSI-A5LV Serial number
GLT5016BSI-ABM-NUN-BUE	ES	415-pin µPGA package. VIS version.12bit,500kHz,108pairs@960M. Sealed D263® Teco glass lid with AR coating on both sides.	GLT5016BSI-A5LV Serial number
GLT5016BSI-ABM-MUN-BUD	Demo	415-pin µPGA package. VIS version.10bit,500kHz,72pairs@1.2G. Sealed D263® Teco glass lid with AR coating on both sides.	GLT5016BSI-A5LV M Serial number
GLT5016BSI-ABM-MUN-BUE	ES	415-pin µPGA package. VIS version.10bit,500kHz,72pairs@1.2G. Sealed D263® Teco glass lid with AR coating on both sides.	GLT5016BSI-A5LV M Serial number
GLT5016BSI-AUM-NUN-BRD	Demo	415-pin µPGA package. UV version. 12bit,500kHz,108pairs@960M. Removable D263® Teco glass lid with AR coating on both sides.	GLT5016BSI-A5LU-R Serial number
GLT5016BSI-AUM-NUN-BRE	ES	415-pin µPGA package. UV version. 12bit,500kHz,108pairs@960M. Removable D263® Teco glass lid with AR coating on both sides.	GLT5016BSI-A5LU-R Serial number
GLT5016BSI-AUM-MUN-BRD	Demo	415-pin µPGA package. UV version. 10bit,500kHz,72pairs@1.2G. Removable D263® Teco glass lid with AR coating on both sides.	GLT5016BSI-A5LU-R M Serial number
GLT5016BSI-AUM-MUN-BRE	ES	415-pin µPGA package. UV version. 10bit,500kHz,72pairs@1.2G. Removable D263® Teco glass lid with AR coating on both sides.	GLT5016BSI-A5LU-R M Serial number

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